PAGE	TITLE
01	INDEX
02	BLOCK DIAGRAM
03	CLOCKS DIAGRAM
04	POWER DISTRIBUTION DIAGRAM
05	POWER FLOW DIAGRAM
06	STRAP & GPIO
07	POWER SEQUENCE DIAGRAM
08	INTERRUPT & PME DIAGRAM
09	CPU XDP
10	MCP- CLK/CTRL/MISC/DEBUG
11	MCP- DDR4 CHANNEL A & B
12	MCP- PCI/DMI/DDI
13	MCP- POWER CONNECTIONS
14	MCP- VSS
15	DDR4 CHA D0 XIMM4
16	DDR4 CHA D1 XIMM3
17	DDR4 CHB D0 XIMM2
18	DDR4 CHB D1 XIMM1
19	DDR RESET
20	PCH - (E)SPI/HDA/SMB/GPIO
21	PCH - GPIO/MISC
22	PCH - CLOCK
23	PCH - PWR/STRAP
24	PCH-PLL FILTER & DECOUPLING
25	SIO_1
26	SIO_2
27	SIO_3
28	SIO_4
29	SIO_5
30	BLANK
31	LEGACY-IO
32	ENT15 USBC Header
33	TPM
34	BIOS
35	FAN HEADERS
36	PCIE - x16
37	DISPLAY PORT 1
38	M2_2230_SOCKET1-KEYE
39	Security
40	Battery/CMOS
41	PWR CON/AUXLED
42	PLATFORM DEBUG
43	LEDs/METS
44	D8D6_CCG4 Controller
45	D8D6_Intel Jacksonville
46	D8D6_USB CHARGER
47	D8D6_USB POWER
48	BLANK
49	D8D6_DISPLAY PORT 2
50	D8D6_HOOD SENSE
51	D8D6_Single COM Port
52	D8D6_Rear Option Card
53	D8D6_NC NET TEST POINT
54	D8_CLINK Header
55	Input Current Monitor
56	Input PSU ID
57	UVP
58	System Power
59	+5V_GPIO
60	+1.8V_AUX
61	+1V_PCH
62	+VPP
63	+1P2V_VDDQ
64	+VTT_DDR
65	+12V_MAIN
66	+5V_MAIN & +3P3V_MAIN
67	+VCCIO
68	+VCCSA
69	+VCCIA CONTROLLER
70	+VCORE PHASE 1 & 2
71	+VCORE PHASE 3
72	+VGT Phase 1 & 2

PAGE	TITLE
73	BLANK
74	COMMON-PCH-DMI/PCIE/USB2-3
75	COMMON-PCH-SATA/PCIE/GPIO
76	COMMON-F-USB2-REDRIVER
77	COMMON-PWRBTN/SATA POWER
78	COMMON-AUDIO CODEC
79	COMMON-F-AUDIO
80	COMMON-PCIE - x4(SLOT4)
81	COMMON-PCIE - x1(SLOT2)
82	COMMON-HLOCK-THMAL SENSOR
83	COMMON-REAR USB3.1x4
84	COMMON-RJ45+USB2/INT-USB3
85	APUS_R-LINE IN OUT
86	APUS_F-TYPEC-REDRIVER
87	APUS_F-USB3.1
88	APUS_F-USB2.0/F-PANEL
89	APUS_F-HEADPHONE
90	APUS_PCIE - x1(SLOT3)
91	APUS_SATA
92	APUS_PCB/EMI CAP
93	APUS_M.2 2280-3M-FT ONLY
	Changelist_EE
	Changelist_PWR

Intel KabyLake Platform

KabyLake S CPU / KabyLake PCH-H

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PCA P/N	901014-001	901017-001	901195-001	901192-001	901006-001	901010-001
SCH P/N	901015-000	901018-000	901196-000	901193-000	901007-000	901011-000
PCB P/N	901016-001	901019-001	901197-001	901194-001	901008-001	901012-001
PCB P/N	Q270	Q270	Q270	Q270		

Marking	Description
I	Installed
NI	Not Installed
MP	Production Part ONLY
PROTO	Not For Production Part
CCL	Critical Components List

PCB AND SILKSCREEN COLOR

Program Phase	Color of PCB	Silkscreen
DB1 (Design Build)	RED	YELLOW
DB2+	RED	WHITE
SI1 (System Integration)	LIGHT BLUE	YELLOW
SI2+	LIGHT BLUE	WHITE
PV1 (Production Validation)	GREEN	YELLOW
PV2+	GREEN	WHITE
MVB / PRODUCTION	GREEN	WHITE

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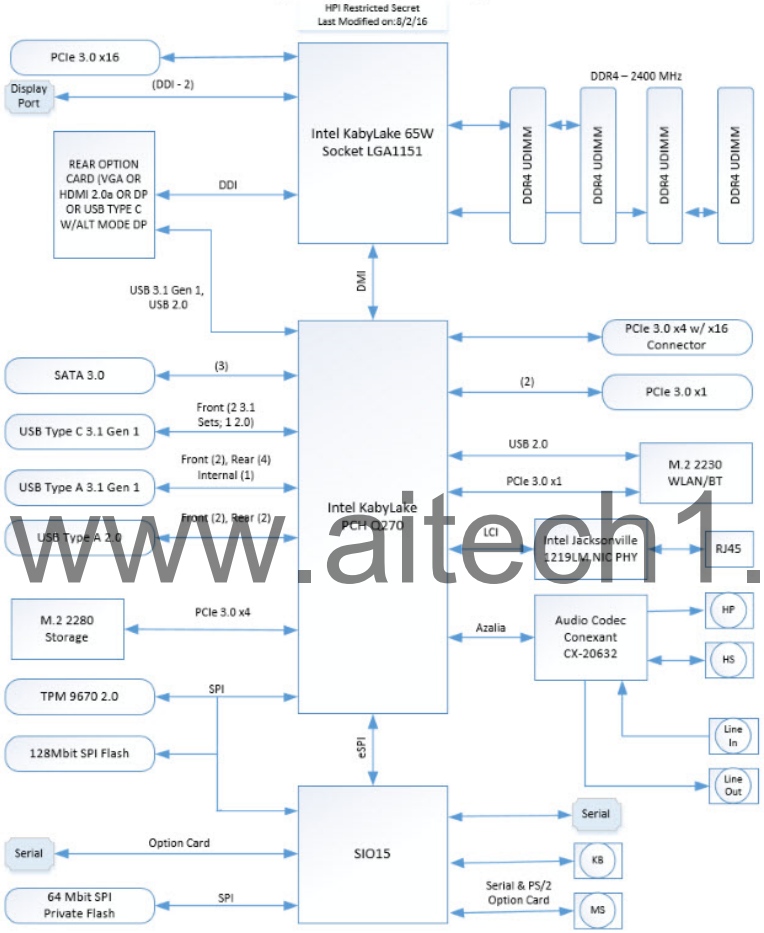
Date: Wednesday, November 09, 2016 | Sheet 1 of 92

Apus 800 G3 SFF Block Diagram

HPI Restricted Secret
Last Modified on:8/2/16



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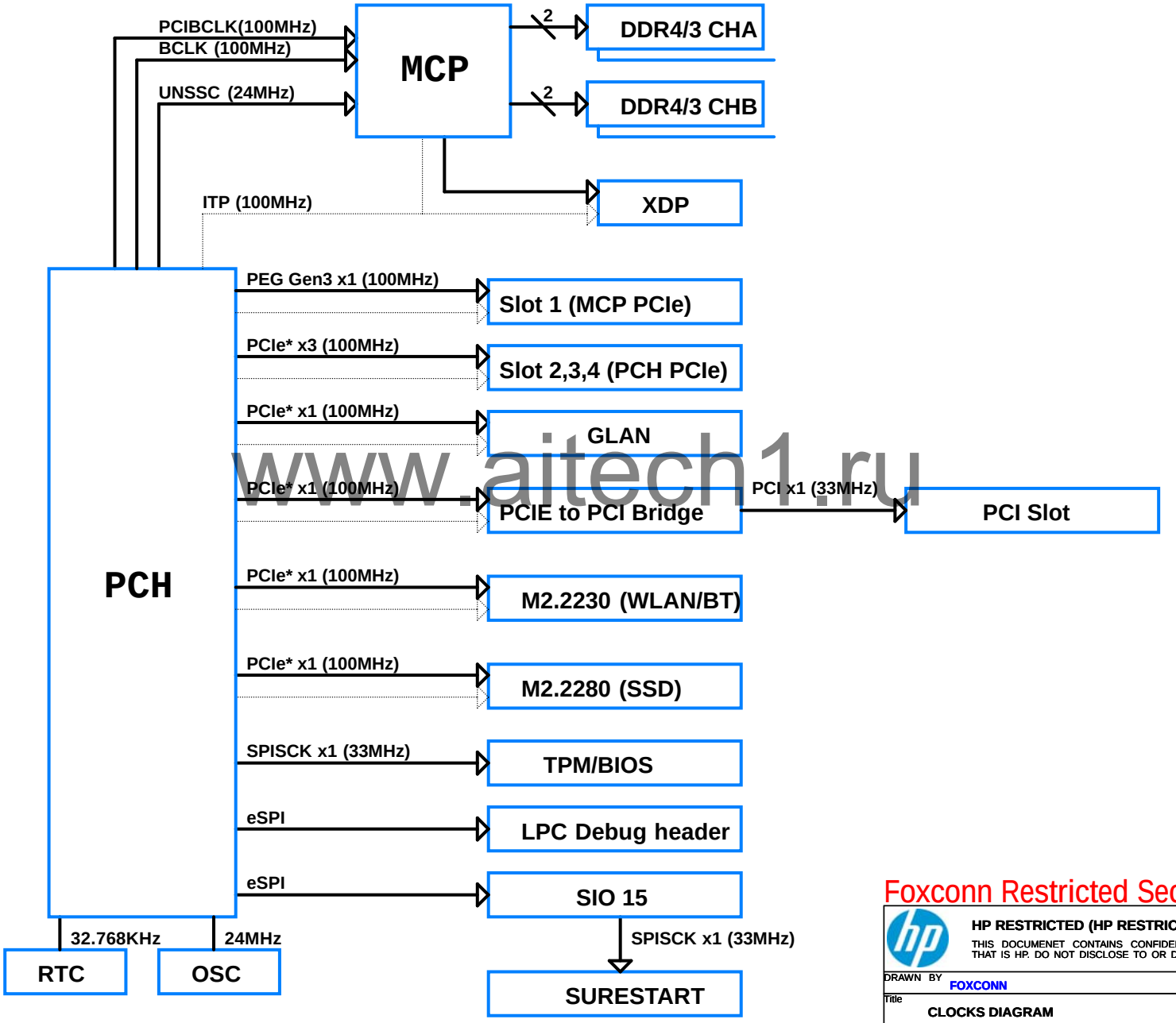
Title: BLOCK DIAGRAM

Size	Document Number	Rev
Custom	901015-000	A

Date: Wednesday, November 09, 2016 | Sheet 2 of 92

Clock Diagram



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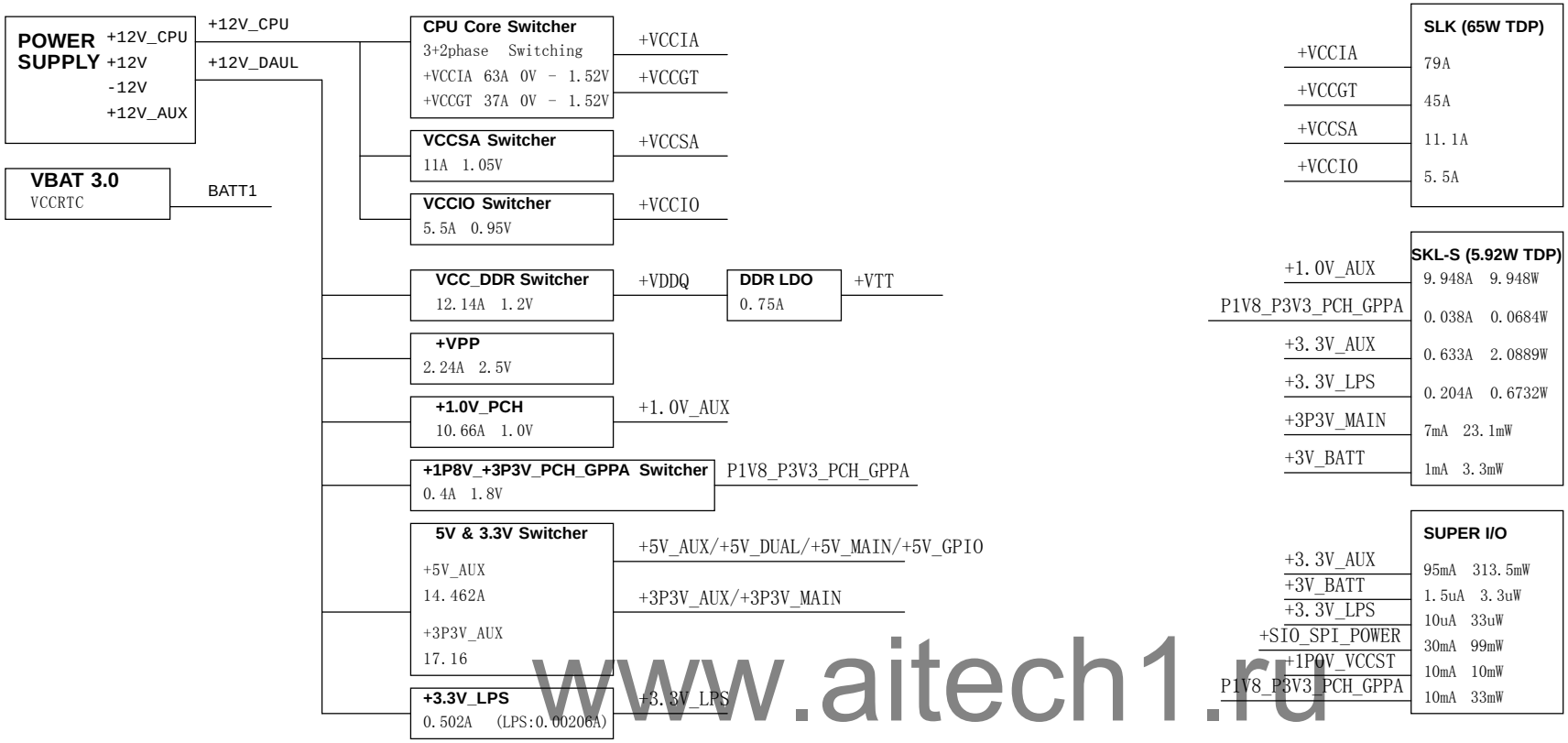
Title	CLOCKS DIAGRAM		
Size: Custom	Document Number: 901015-000		Rev: A
Date: Wednesday, November 09, 2016	Sheet 3 of 92		



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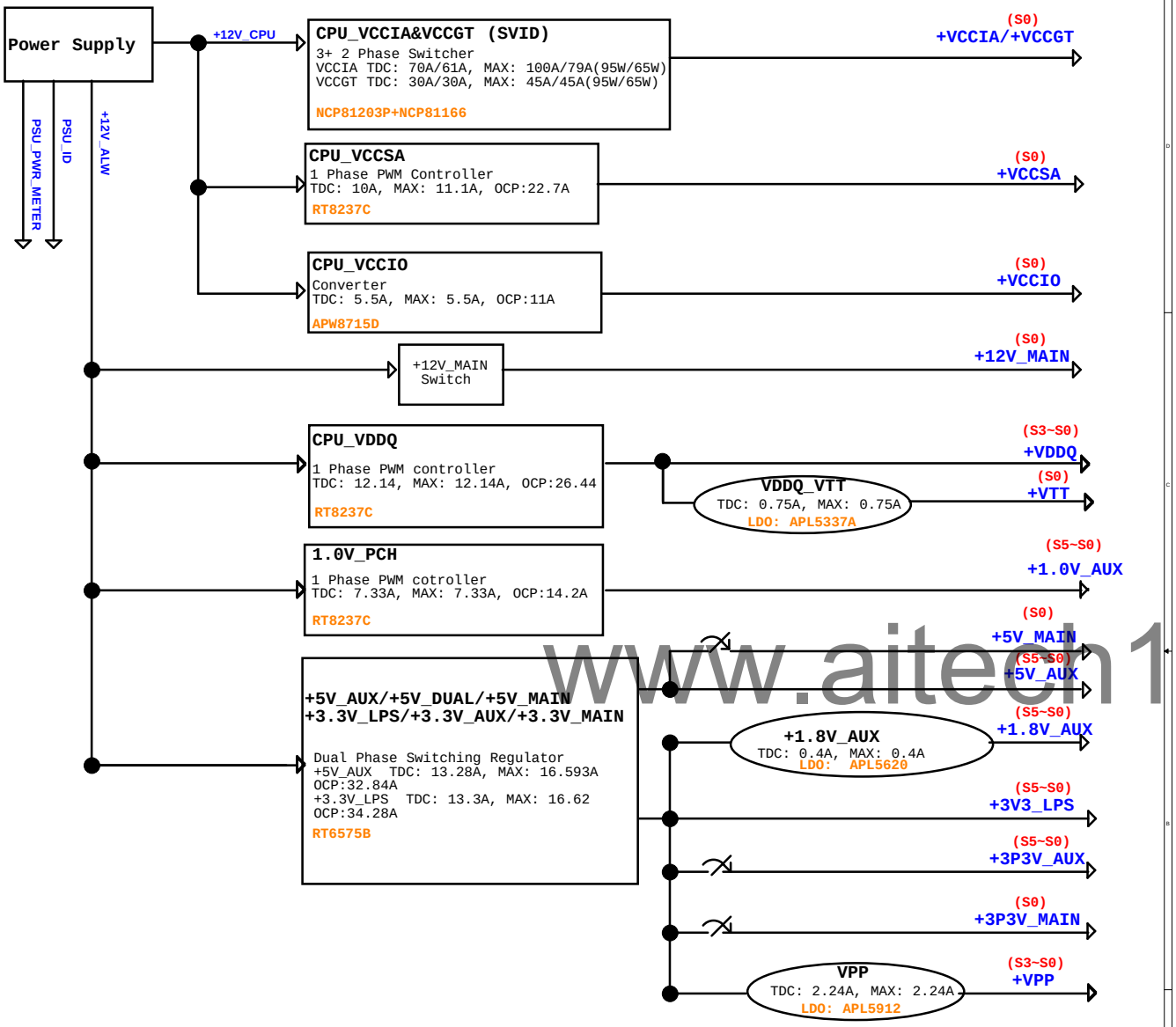
Title: POWER DISTRIBUTION DIAGRAM

Size: Custom | Document Number: 901015-000 | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 4 of 92



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Title: POWER FLOW

Size: Custom | Document Number: 901015-000 | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 5 of 101

	Intel PU/PD (Note1)	NMI or SMI	Multiplexed with	Defalut	Native, GP or Alternative	I/O	Output Level	Strap Function	Function
GPP_A0	None	None	LPC mode : RCIN# eSPI mode : None	LPC mode : RCIN# eSPI mode : GPI	N	I	-	None	Not Used
GPP_A1	None	None	LPC mode : LAD0 eSPI mode : eSPI_IO0	LPC mode : LAD0 eSPI mode : eSPI_IO0	N	I/O	3.3V	None	ESPI_IO0
GPP_A2	None	None	LPC mode : LAD1 eSPI mode : eSPI_IO1	LPC mode : LAD1 eSPI mode : eSPI_IO1	N	I/O	3.3V	None	ESPI_IO1
GPP_A3	None	None	LPC mode : LAD2 eSPI mode : eSPI_IO2	LPC mode : LAD2 eSPI mode : eSPI_IO2	N	I/O	3.3V	None	ESPI_IO2
GPP_A4	None	None	LPC mode : LAD3 eSPI mode : eSPI_IO3	LPC mode : LAD3 eSPI mode : eSPI_IO3	N	I/O	3.3V	None	ESPI_IO3
GPP_A5	None	None	LPC mode : LFRAME eSPI mode : eSPI_CS#	LPC mode : LFRAME eSPI mode : eSPI_CS#	N	O	3.3V	None	eSPI_CS#
GPP_A6	None	None	LPC mode : SERIRQ eSPI mode : None	LPC mode : SERIRQ eSPI mode : GPI	N	O	3.3V	None	Not Used
GPP_A7	None	None	LPC mode : PIRQA# eSPI mode : None	LPC mode : PIRQA# eSPI mode : GPI	N	O	3.3V	None	Not Used
GPP_A8	None	None	LPC mode : CLKRUN# eSPI mode : None	LPC mode : CLKRUN# eSPI mode : GPI	N	O	3.3V	None	Not Used
GPP_A9	None	None	LPC mode : CLKOUT_0 eSPI mode : eSPI_CLK	LPC mode : CLKOUT_0 eSPI mode : eSPI_CLK	N	O	3.3V	None	eSPI_CLK
GPP_A10	None	None	LPC mode : CLKOUT_1 eSPI mode : None	LPC mode : CLKOUT_1 eSPI mode : GPI	N	O	3.3V	None	Not Used
GPP_A11	None	None	LPC mode : PME# eSPI mode : None	LPC mode : PME# eSPI mode : GPI	N	I	-	None	GPI (eSPI)
GPP_A12	None	None	BM_BUSY#/ISH_GP6	GPI	A	I	-	None	SX_EXIT_HOLDOFF_N
GPP_A13	None	None	LPC mode : SUSWARN#/SUSPWRDNACK eSPI mode : None	LPC mode : SUSWARN#/SUSPWRDNACK eSPI mode : GPI	N	O	3.3V	None	GPI (eSPI)
GPP_A14	None	None	LPC mode : SUS_STAT# eSPI mode : eSPI_RESET#	LPC mode : SUS_STAT# eSPI mode : eSPI_RESET#	N	O	3.3V	None	eSPI_RESET#
GPP_A15	None	None	LPC mode : SUS_ACK# eSPI mode : None	LPC mode : SUS_ACK# eSPI mode : GPI	N	I	-	None	GPI (eSPI)
GPP_A16	None	None	SD_1P8_SEL	GPI	N	I(*)	-	None	Not Used
GPP_A17	None	None	SD_PWR_EN#/ISH_GP7	GPI	N	I(*)	-	None	Not Used
GPP_A18	None	None	ISH_GP0	GPI	N	I(*)	-	None	Not Used
GPP_A19	None	None	ISH_GP1	GPI	N	I(*)	-	None	Not Used
GPP_A20	None	None	ISH_GP2	GPI	N	I(*)	-	None	Not Used
GPP_A21	None	None	ISH_GP3	GPI	N	I(*)	-	None	Not Used
GPP_A22	None	None	ISH_GP4	GPI	N	I(*)	-	None	Not Used
GPP_A23	None	None	ISH_GP5	GPI	N	I(*)	-	None	Not Used

I(*) means need to enable the internal PD by BIOS

	Intel PU/PD (Note1)	NMI or SMI	Multiplexed with	Defalut	Native, GP or Alternative	I/O	Output Level	Strap Function	Function
GPP_D0	None	NMI SMI	SPI1_CS#	GPI	N	I(*)	-	None	Not Used
GPP_D1	None	NMI SMI	SPI1_CLK	GPI	N	I(*)	-	None	Not Used
GPP_D2	None	NMI SMI	SPI1_MISO_IO1	GPI	N	I(*)	-	None	Not Used
GPP_D3	None	NMI SMI	SPI1_MISO_IO0	GPI	N	I(*)	-	None	Not Used
GPP_D4	None	NMI SMI	ISH_I2C2_SDA	GPI	N	I(*)	-	None	Not Used
GPP_D5	None	None	SSP0_SFRM	GPI	N	I(*)	-	None	Not Used
GPP_D6	None	None	SSP0_TXD	GPI	N	I(*)	-	None	Not Used
GPP_D7	None	None	SSP0_RXD	GPI	N	I(*)	-	None	Not Used
GPP_D8	None	None	SSP0_SCLK	GPI	N	I(*)	-	None	Not Used
GPP_D9	None	None	ISH_SPI_CS#	GPI	N	I(*)	-	None	Not Used
GPP_D10	None	None	ISH_SPI_CLK	GPI	N	I(*)	-	None	Not Used
GPP_D11	None	None	ISH_SPI_MISO	GPI	N	I(*)	-	None	Not Used
GPP_D12	None	None	ISH_SPI_MOSI	GPI	N	I(*)	-	None	Not Used
GPP_D13	None	None	ISH_UART0_RXD	GPI	N	I(*)	-	None	Not Used
GPP_D14	None	None	ISH_UART0_TXD	GPI	N	I(*)	-	None	Not Used
GPP_D15	None	None	ISH_UART0_RTS#	GPI	N	I(*)	-	None	Not Used
GPP_D16	None	None	ISH_UART0_CTS#	GPI	N	I(*)	-	None	Not Used
GPP_D17	None	None	DMIC_CLK1	GPI	N	I(*)	-	None	Not Used
GPP_D18	None	None	DMIC_DATA1	GPI	N	I(*)	-	None	Not Used
GPP_D19	None	None	DMIC_CLK0	GPI	N	I(*)	-	None	Not Used
GPP_D20	None	None	DMIC_DATA0	GPI	N	I(*)	-	None	Not Used
GPP_D21	None	None	SPI1_IO2	GPI	N	I(*)	-	None	Not Used
GPP_D22	None	None	SPI1_IO3	GPI	N	I(*)	-	None	Not Used
GPP_D23	None	None	ISH_I2C2_SCL	GPI	N	I(*)	-	None	Not Used

I(*) means need to enable the internal PD by BIOS

	Intel PU/PD (Note1)	NMI or SMI	Multiplexed with	Defalut	Native, GP or Alternative	I/O	Output Level	Strap Function	Function
GPP_G0	None	None	None	GPI	N	I(*)	-	None	Not Used
GPP_G1	None	None	None	GPI	N	I(*)	-	None	Not Used
GPP_G2	None	None	None	GPI	N	I(*)	-	None	Not Used
GPP_G3	None	None	None	GPI	N	I	-	None	TBT_CABLE_DET#(WS)
GPP_G4	None	None	None	GPI	N	I(*)	-	None	Not Used
GPP_G5	None	None	None	GPI	N	I(*)	-	None	Not Used
GPP_G6	None	None	None	GPI	G	I	-	None	HPGP_BOOT_BLK_EN#
GPP_G7	None	None	None	GPI	N	I(*)	-	None	Not Used
GPP_G8	None	None	None	GPI	N	I(*)	-	None	Not Used
GPP_G9	None	None	None	GPI	N	I	-	None	HPGP_HOOD_SW_DET#
GPP_G10	None	None	None	GPI	G	I	-	None	HPGP_PASSWORD_EN
GPP_G11	None	None	None	GPI	G	I	-	None	HPGP_HOOD_LOCK_DET
GPP_G12	None	None	GSXDOUT	GPI	G	I	-	None	HPGP_Front_USB3.0_DET#1
GPP_G13	None	None	GSXSLOAD	GPI	N	I(*)	-	None	HPGP_FRONT_USB2.0_DET#1
GPP_G14	None	None	GSXDIN	GPI	N	I	-	None	HPGP_FRONT_USB2.0_DET#0 (charging)
GPP_G15	None	None	GSXRESET#	GPI	N	I	-	None	HPGP_INT_USB3.0_DET#0
GPP_G16	None	None	GSXCLK	GPI	N	I	-	None	HPGP_FRONT_AUDIO_DET#
GPP_G17	None	None	ADR_COMPLETE	GPI	N	I	-	None	HPGP_REAR_SERIAL_DET#0
GPP_G18	None	None	NMI#	GPI	N	I(*)	-	None	PCH_GPP_G18_NMI#
GPP_G19	None	None	SMI#	GPI	N	I	-	None	INT_USB_DET2# (WS)
GPP_G20	None	None	None	GPI	N	I(*)	-	None	None
GPP_G21	None	None	None	GPI	N	I	-	None	SPI_TPM_PIRQ
GPP_G22	None	None	None	GPI	G	I	-	None	TBT_FRC_PWR(WS)
GPP_G23	None	None	None	GPI	G	I	-	None	TBT_PLUG_EVENT(WS)

I(*) means need to enable the internal PD by BIOS

	Intel PU/PD (Note1)	NMI or SMI	Multiplexed with	Defalut	Native, GP or Alternative	I/O	Output Level	Strap Function	Function
GPD0	None	None	BATLOW#	BATLOW#	G	I(*)	-	None	Not Used
GPD1	None	None	ACPRESENT	ACPRESENT	N	O	3.3V	None	ACPRESENT
GPD2	None	None	LAN_WAKE#	LAN_WAKE#	N	I	-	None	LAN_WAKE#
GPD3	None	None	PWRBTN#	PWRBTN#	N	I	-	None	PWRBTN#
GPD4	None	None	SLP_S3#	SLP_S3#	N	O	3.3V	None	SLP_S3#
GPD5	None	None	SLP_S4#	SLP_S4#	N	O	3.3V	None	SLP_S4#
GPD6	None	None	SLP_A#	SLP_A#	N	O	3.3V	None	SLP_A#
GPD7	None	None	USB_WAKEOUT#	USB_WAKEOUT#	G	I(*)	-	None	Not Used
GPD8	None	None	SUS_CLK	SUS_CLK	N	O	3.3V	None	SUS_CLK
GPD9	None	None	SLP_WLAN#	SLP_WLAN#	G	I(*)	-	None	Not Used
GPD10	None	None	SLP_S5#	SLP_S5#	N	O	3.3V	None	SLP_S5#
GPD11	None	None	LANPHYPC	LANPHYPC	G	I	-	None	HPGP_LAN_DISABLE#

I(*) means need to enable the internal PD by BIOS

	Intel PU/PD (Note1)	NMI or SMI	Multiplexed with	Defalut	Native, GP or Alternative	I/O	Output Level	Strap Function	Function
GPP_B0	None	None	None	GPO	G	I(*)	-	None	Not Used
GPP_B1	None	None	None	GPO	N	I(*)	-	None	Not Used
GPP_B2	None	None	VRALERT#	GPI	N	I(*)	-	None	Not Used
GPP_B3	None	None	CPU_GP2	GPI	N	I(*)	-	None	Not Used
GPP_B4	None	None	CPU_GP3	GPI	N	I(*)	-	None	Not Used
GPP_B5	None	None	SRCCLKREQ0#	GPI	N	I(*)	-	None	Not Used
GPP_B6	None	None	SRCCLKREQ1#	GPI	N	I(*)	-	None	Not Used
GPP_B7	None	None	SRCCLKREQ2#	GPI	N	I(*)	-	None	Not Used
GPP_B8	None	None	SRCCLKREQ3#	GPI	N	I(*)	-	None	Not Used
GPP_B9	None	None	SRCCLKREQ4#	GPI	N	I(*)	-	None	Not Used
GPP_B10	None	None	SRCCLKREQ5#	GPI	N	I(*)	-	None	Not Used
GPP_B11	None	None	EXIT_PWR_GATE#	GPI	N	I(*)	-	None	Not Used
GPP_B12	None	None	SLP_S0#	SLP_S0#	N	O	3.3V	None	Reserved
GPP_B13	None	None	PLTRST#	PLTRST#	N	O	3.3V	None	PLTRST#
GPP_B14	20K PD	NMI SMI	SPKR	GPO	A	O	3.3V	BOOT_BL_REC	SPKR
GPP_B15	None	None	GSPIO_CS#	GPI	N	I(*)	-	None	BOOT_BL_REC
GPP_B16	None	None	GSPIO_CLK	GPI	N	I(*)	-	None	Not Used
GPP_B17	None	None	GSPIO_MISO	GPI	N	I(*)	-	None	Not Used
GPP_B18	20K PD	None	GSPIO_MOSI	GPO	N	I(*)	-	NO REBOOT	Strap Pin
GPP_B19	None	None	GSPI1_CS#	GPI	N	I(*)	-	None	Not Used
GPP_B20	None	NMI SMI	GSPI1_CLK	GPI	N	I(*)	-	None	Not Used
GPP_B21	None	None	GSPI1_MISO	GPI	N	I(*)	-	None	Not Used
GPP_B22	20K PD	None	GSPI1_MOSI	GPO	N	I(*)	-	BOOT BIOS STRAP	Strap Pin
GPP_B23	20K PD	NMI SMI	SML1ALERT#/ PCHHOT#	GPO	N	I(*)	-	EXI BOOT STALLBYPASS STRAP	Strap Pin

I(*) means need to enable the internal PD by BIOS

	Intel PU/PD (Note1)	NMI or SMI	Multiplexed with	Defalut	Native, GP or Alternative	I/O	Output Level	Strap Function	Function
GPP_E0	None	NMI SMI	SATAXPCIE0/ SATAGP0	SATAXPCIE0/ SATAGP0 or GPI	N	I(*)	-	None	Not Used
GPP_E1	None	NMI SMI	SATAXPCIE1/ SATAGP1	SATAXPCIE1/ SATAGP1 or GPI	N	I(*)	-	None	Not Used
GPP_E2	None	NMI SMI	SATAXPCIE2/ SATAGP2	SATAXPCIE2/ SATAGP2 or GPI	N	I(*)	-	None	Not Used
GPP_E3	None	NMI SMI	CPU_GP0	GPI	N	I(*)	-	None	Not Used
GPP_E4	None	NMI SMI	SATA_DEVSLP0	GPI	N	I(*)	-	None	Not Used
GPP_E5	None	NMI SMI	SATA_DEVSLP1	GPI	N	I(*)	-	None	Not Used
GPP_E6	None	NMI SMI	SATA_DEVSLP2	GPI	N	I(*)	-	None	Not Used
GPP_E7	None	NMI SMI	CPU_GP1	GPI	N	I(*)	-	None	Not Used
GPP_E8	None	NMI SMI	SATA_LED#	GPI	A	O	-	None	SATA_LED#
GPP_E9	20K PD	None	USB_OC0#	GPI	G	I	-	None	USB_OC#
GPP_E10	20K PD	None	USB_OC1#	GPI	G	I	-	None	USB_OC#
GPP_E11	20K PD	None	USB_OC2#	GPI	G	I	-	None	USB_OC#
GPP_E12	20K PD	None	USB_OC3#	GPI	N	I(*)	-	None	Not Used

I(*) means need to enable the internal PD by BIOS

	Intel PU/PD (Note1)	NMI or SMI	Multiplexed with	Defalut	Native, GP or Alternative	I/O	Output Level	Strap Function	Function
GPP_H0	None	None	SCRCLKRES6#	GPI	N	I(*)	-	None	Not Used
GPP_H1	None	None	SCRCLKRES7#	GPI	N	I	-	None	HPGP_STD_PSU_DET#
GPP_H2	None	None	SCRCLKRES8#	GPI	N	I	-	None	HPGP_PCI_EXT_DET#
GPP_H3	None	None	SCRCLKRES9#	GPI	N	I	-	None	HPGP_CLINK_DET#
GPP_H4	None	None	SCRCLKRES10#	GPI	N	I	-	None	LAN_CLKREQ#
GPP_H5	None	None	SCRCLKRES11#	GPI	N	I(*)	-	None	Not Used
GPP_H6	None	None	SCRCLKRES12#	GPI	N	I	-	None	M.2_CLKREQ#(WS)
GPP_H7	None	None	SCRCLKRES13#	GPI	N	I(*)	-	None	Not Used
GPP_H8	None	None	SCRCLKRES14#	GPI	N	I(*)	-	None	HPGP_DPCARD_DET#
GPP_H9	None	None	SCRCLKRES15#	GPI	N	I(*)	-	None	Not Used
GPP_H10	None	None	None	GPI	G	I	-	None	HPGP_WRITE_EDID_ROM
GPP_H11	None	None	None	GPO	N	I(*)	-	None	Not Used
GPP_H12	20K PD	None	None	GPI	N	I(*)	-	ESPI Flash Sharing Mode Strape	PCH_STRAP_GPP_H12
GPP_H13	20K PD	None	None	GPI	N	I(*)	-	None	Not Used
GPP_H14	None	None	None	GPI	N	I	-	None	HPGP_FPR _PRESENT#
GPP_H15	None	None	None	GPI	N	I(*)	-	None	Not Used
GPP_H16	None	None	None	GPI	N		-	None	HPGP_FPR_OFF
GPP_H17	None	None	None	GPI	N		-	None	HPGP_FPR_LOCK#
GPP_H18	None	None	None	GPI	N	I	-	None	Not Used
GPP_F19	None	None	ISH_I2C0_SDA	GPI	N	I	-	None	HPGP_TPNL_PRESENT#
GPP_H20	None	None	ISH_I2C0_SCL	GPI	N	I	-	None	HPGP_LegucyIO_PRESENT#
GPP_H21	None	None	ISH_I2C1_SDA	GPI	N	I	-	None	HPGP_CVTR_PRESENT#
GPP_H22	None	None	ISH_I2C1_SDL	GPI	N	I	-	None	HPGP_WEBCAM_PRESENT#
GPP_H23	None	None	None	GPI	N	I	-	None	HPGP_LVDS/eDP_PRESENT#

I(*) means need to enable the internal PD by BIOS

	Intel PU/PD (Note1)	NMI or SMI	Multiplexed with	Defalut	Native, GP or Alternative	I/O	Output Level	Strap Function	Function
GPP_C0	None	None	SMB_CLK	SMB_CLK	N	O	-	None	SMBCLK
GPP_C1	None	None	SMB_DATA	SMB_DATA	N	I/O	-	None	SMBDATA
GPP_C2	20K PD	None	SMBALERT#	GPO	N	I(*)	-	(TLS Strap) PCH_STRAP_TLS	PCH_STRAP_TLS
GPP_C3	None	None	SML0CLK	SML0CLK	N	O	-	None	SML0CLK
GPP_C4	None	None	SML0DATA	SML0DATA	N	I/O	-	None	SML0DATA
GPP_C5	20K PD	None	SML0ALERT#	GPO	N	I(*)	-	ESPI ENABLE STRAP	PCH_STRAP_ESPI_EN
GPP_C6	None	None	SML1CLK	GPI	A	I(*)	-	None	SML1CLK_PCH
GPP_C7	None	None	SML1DATA	GPI	A	I(*)	-	None	SML1DATA_PCH
GPP_C8	None	None	UART0_RXD	GPI	N	I(*)	-	None	Not Used
GPP_C9	None	None	UART0_TXD	GPI	N	I(*)	-	None	Not Used
GPP_C10	None	None	UART0_RTS#	GPI	N	I(*)	-	None	Not Used
GPP_C11	None	None	UART0_CTS#	GPI	N	I(*)	-	None	Not Used
GPP_C12	None	None	UART1_RXD/ ISH_UART1_RXD	GPI	N	I(*)	-	None	Not Used
GPP_C13	None	None	UART1_TXD/ ISH_UART1_TXD	GPI	N	I(*)	-	None	Not Used
GPP_C14	None	None	UART1_RTS#/ ISH_UART1_RTS#	GPI	N	I(*)	-	None	Not Used
GPP_C15	None	None	UART1_CTS#/ ISH_UART1_CTS#	GPI	N	I(*)	-	None	Not Used
GPP_C16	None	None	I2SC0_SCA	GPI	N	I(*)	-	None	Not Used
GPP_C17	None	None	I2SC0_SCL	GPI	N	I(*)	-	None	Not Used
GPP_C18	None	None	I2SC1_SDA	GPI	N	I(*)	-	None	Not Used
GPP_C19	None	None	I2SC1_SDL	GPI	N	I(*)	-	None	Not Used
GPP_C20	None	None	UART2_RXD	GPI	N	I(*)	-	None	Not Used
GPP_C21	None	None	UART2_TXD	GPI	N	I(*)	-	None	Not Used
GPP_C22	None	NMI SMI	UART2_RTS#	GPI	G	I	-	None	HPGP_SIO_SMI#
GPP_C23	None	NMI SMI	UART2_CTS#	GPI	G	I	-	None	SIO_PME#

I(*) means need to enable the internal PD by BIOS

	Intel PU/PD (Note1)	NMI or SMI	Multiplexed with	Defalut	Native, GP or Alternative	I/O	Output Level	Strap Function	Function
GPP_F0	None	None	SATAXPCIE3/ SATAGP3	SATAXPCIE3/ SATAGP3 or GPI	N	I(*)	-	None	Not Used
GPP_F1	None	None	SATAXPCIE4/ SATAGP4	SATAXPCIE4/ SATAGP4 or GPI	G	I	-	None	M2_PEDET(WS)
GPP_F2	None	None	SATAXPCIE5/ SATAGP5	SATAXPCIE5/ SATAGP5 or GPI	N	I(*)	-	None	Not Used
GPP_F3	None	None	None	GPI	N	I(*)	-	None	Not Used
GPP_F4	None	None	None	GPI	N	O	-	None	HPGP_W_DISABLE#
GPP_F5	None	None	SATA_DEVSLP3	GPI	N	I(*)	-	None	Not Used
GPP_F6	None	None	SATA_DEVSLP4	GPI	N	I	-	None	M2_DEVSLP(WS)
GPP_F7	None	None	SATA_DEVSLP5	GPI	N	I(*)	-	None	Not Used
GPP_F8	None	None	None	GPI	N	I(*)	-	None	Not Used
GPP_F9	None	None	None	GPI	N	I(*)	-	None	Not Used
GPP_F10	None	None	SATA_SCLOCK	GPI	N	I(*)	-	None	Not Used
GPP_F11	None	None	SATA_SCLOAD	GPI	N	I(*)	-	None	Not Used
GPP_F12	None	None	SATA_SDATAOUT1	GPI	N	I(*)	-	None	Not Used
GPP_F13	None	None	SATA_SDATAOUT2	GPI	N	I(*)	-	None	Not Used
GPP_F14	None	None	None	GPI	N	I(*)	-	None	Not Used
GPP_F15	None	None	USB_OC4#	GPI	A	I	-	None	USB_OC#
GPP_F16	None	None	USB_OC5#	GPI	A	I	-	None	USB_OC#
GPP_F17	None	None	USB_OC6#	GPI	A	I	-	None	USB_OC#
GPP_F18	None	None	USB_OC7#	GPI	A	I	-	None	USB_OC#
GPP_F19	None	None	L_VDDEN	GPI	N	I(*)	-	None	Not Used
GPP_F20	None	None	L_BKLTEN	GPI	N	I(*)	-	None	Not Used
GPP_F21	None	None	L_BKLTCTL	GPI	G	I	-	None	L_BKLTCTL
GPP_F22	None	None	None	GPI	N	I(*)	-	None	Not Used
GPP_F23	None	None	None	GPI	N	I(*)	-	None	Not Used

I(*) means need to enable the internal PD by BIOS

	Intel PU/PD (Note1)	NMI or SMI	Multiplexed with	Defalut	Native, GP or Alternative	I/O	Output Level	Strap Function	Function
GPP_I0	None	NMI SMI	DDSP_HPD0	GPI	A	I	-	None	DDSP_HPD0(portB)
GPP_I1	None	NMI SMI	DDSP_HPD1	GPI	A	I	-	None	DDSP_HPD1(portC)
GPP_I2	None	NMI SMI	DDSP_HPD2	GPI	A	I	-	None	DDSP_HPD2(portD)
GPP_I3	None	NMI SMI	DDSP_HPD3	GPI	A	I(*)	-	None	Not Used
GPP_I4	None	None	EDP_HPD	GPI	A	I	-	None	EDP_HPD
GPP_I5	None	None	DDPB_CTRLCLK	GPI	A	I/O	-	None	DDPB_CTRLCLK
GPP_I6	20K PD	None	DDPB_CTRLDATA	GPO	A	I/O	-	None	DDPB_CTRLDATA
GPP_I7	None	None	DDPC_CTRLCLK	GPI	A	I/O	-	None	DDPC_CTRLCLK
GPP_I8	20K PD	None	DDPC_CTRLDATA	GPO	A	I/O	-	None	DDPC_CTRLDATA
GPP_I9	None	None	DDPD_CTRLCLK	GPI	A	I/O	-	None	DDPD_CTRLCLK
GPP_I10	20K PD	None	DDPD_CTRLDATA	GPO	A	I/O	-	None	DDPD_CTRLDATA

I(*) means need to enable the internal PD by BIOS

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Title: STRAP & GPIO

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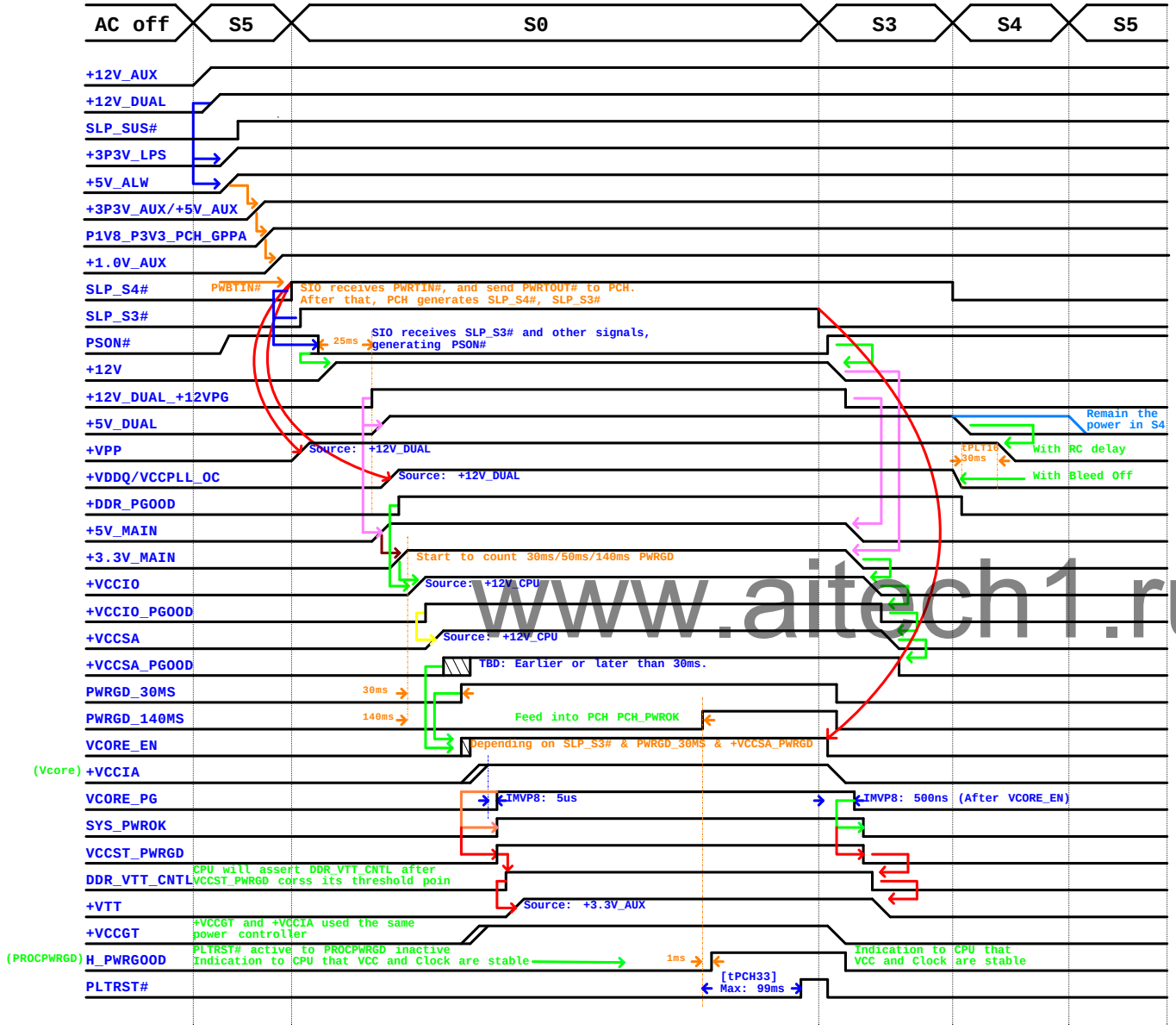
Date: Wednesday, November 09, 2016 | Sheet 6 of 92

POWER SEQUENCE DIAGRAM



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Rev	A
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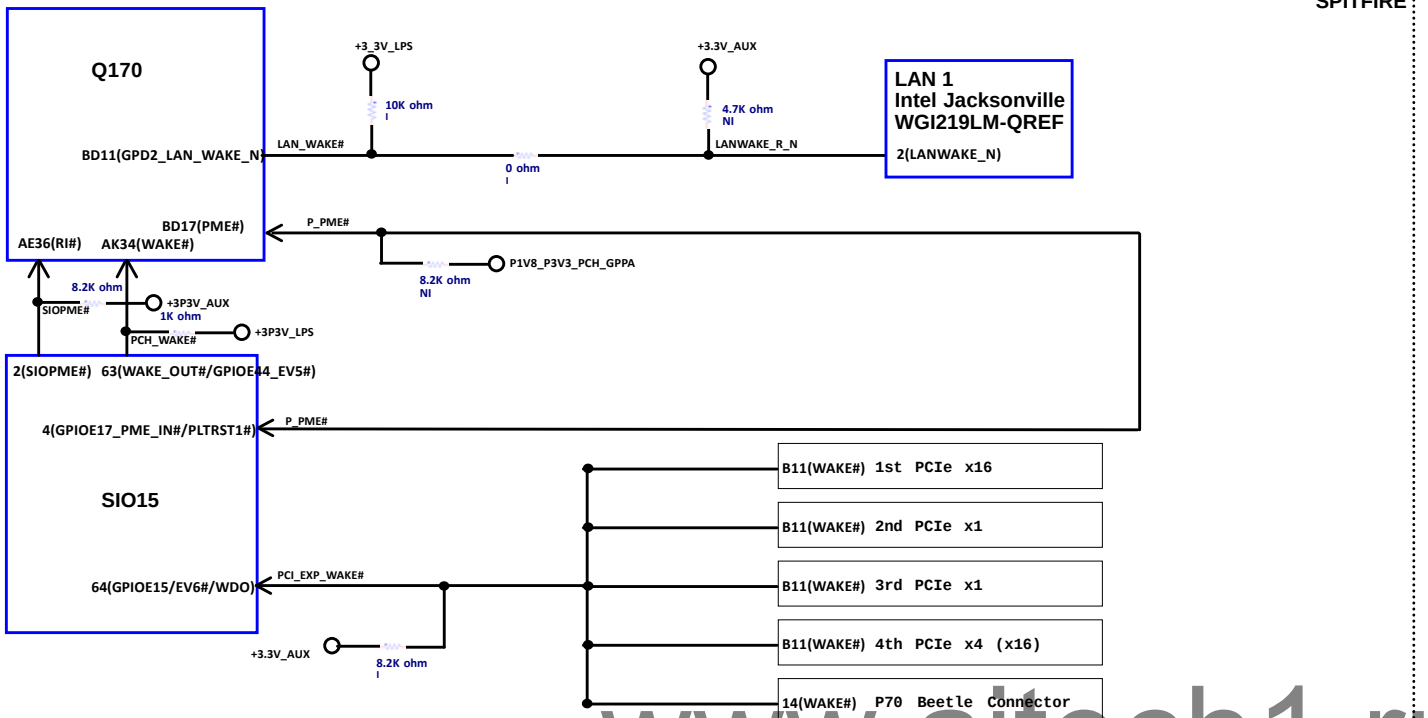
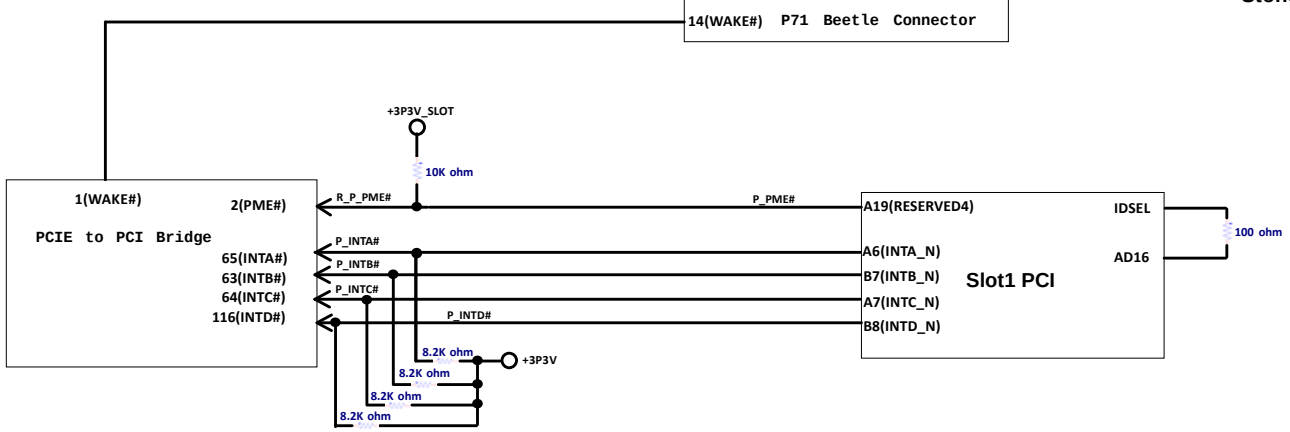
Sheet	7 of 92

Interrupt & PME diagram

SPITFIRE



Stone



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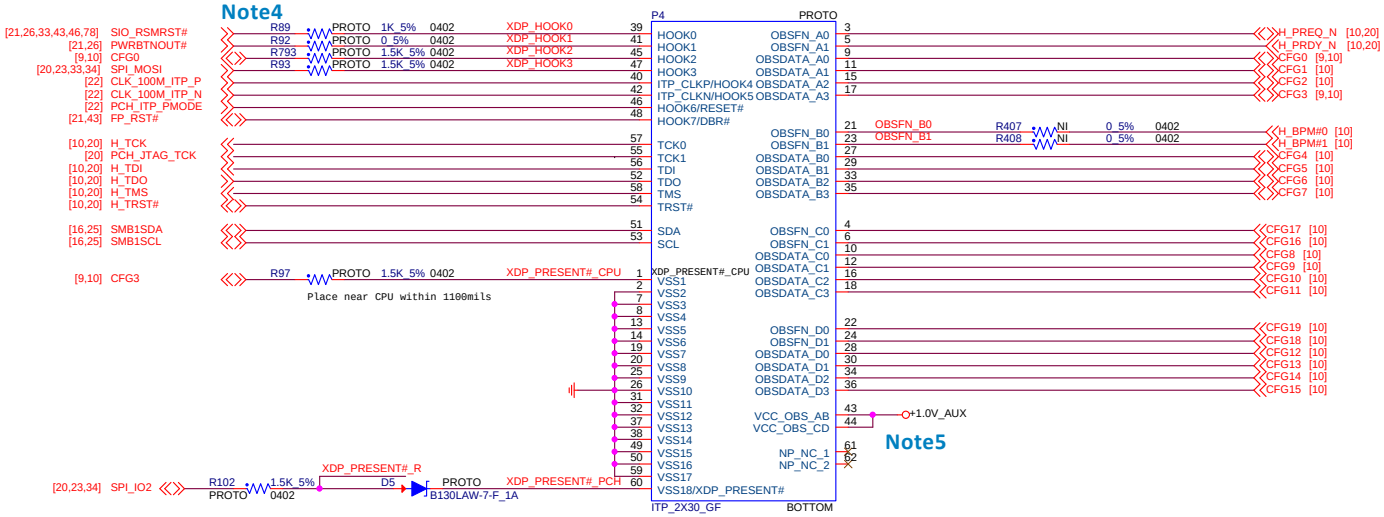
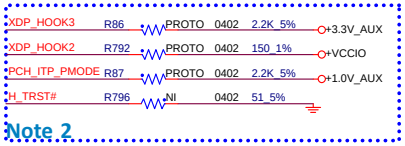
Size / Document Number	Custom 901015-000
Rev	A
Date: Wednesday, November 09, 2016	Sheet 8 of 92

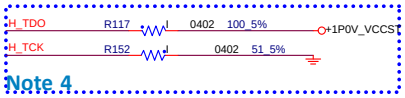
Intel MCP XDP Debug Connector

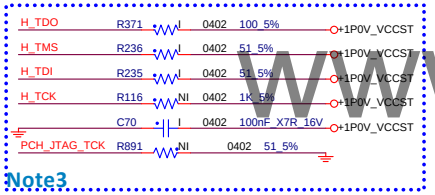
PRDY# and PREQ# must connect for DCI Merged Debug Port Topology



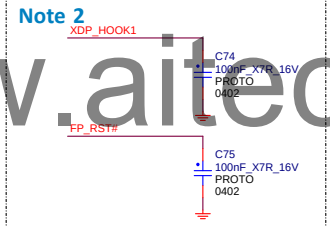
HW PU/PD Configuration







DeCoupling CAP



CFG Connection

BOM Change list for MP PCA if need to enable DCI/XDP:
1.Remove P4 soldermask on pad and install P4 XDP connector.
2.Install D5,R86,R87,R89,R92,R93,R97,R102,R792,R793

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

Design Note

Note 1: XDP Connector Footprint

NPI
HMS2X30CZ
MVB
HMS2X30CZ_MVB_NP

Note 2

C74 Place close to P4 Connector
C75 Place close to P4 Connector
R792 Place close to P4 Connector
R86 Place close to P4 Connector
R87 Place close to P4 Connector
R796 Close P4

Note3

R891 Place Close to U4 Within 1.1"
R116 Place Close to U4 Within 1.1"
R235 Place Close to U4 Within 1.5"
R236 Place Close to U4 Within 1.5"
R371 Place Close to U4 Within 1.5"
C70 Place Close to R235, R236, R371

Note4

R793 Place close to T Point
R89 Place close to T Point
R102 near PCH within 500mils (SPI_IO2)
R93 Close to T-Point of SPI_MOSI < 1100mils
R152 Place Close to CPU Within 1.5"
R117 Place Close to CPU Within 1.5"

Note5

P4.43 and P4.44 Power trace width = 10mils

Note6

R365 should be changed to 1kohm for Hook1 if using XDP, otherwise R365 should be kept as 8.2k. [Power Consumpt i on Concern]

R342 should be changed to 1kohm for Hook7 if using XDP, otherwise R342 should be kept as 10k. [Power Consumpt i on Concern]

E2 Header should install jumper if using XDP, otherwise it should be keep as non-install [Power Sequence Concern]

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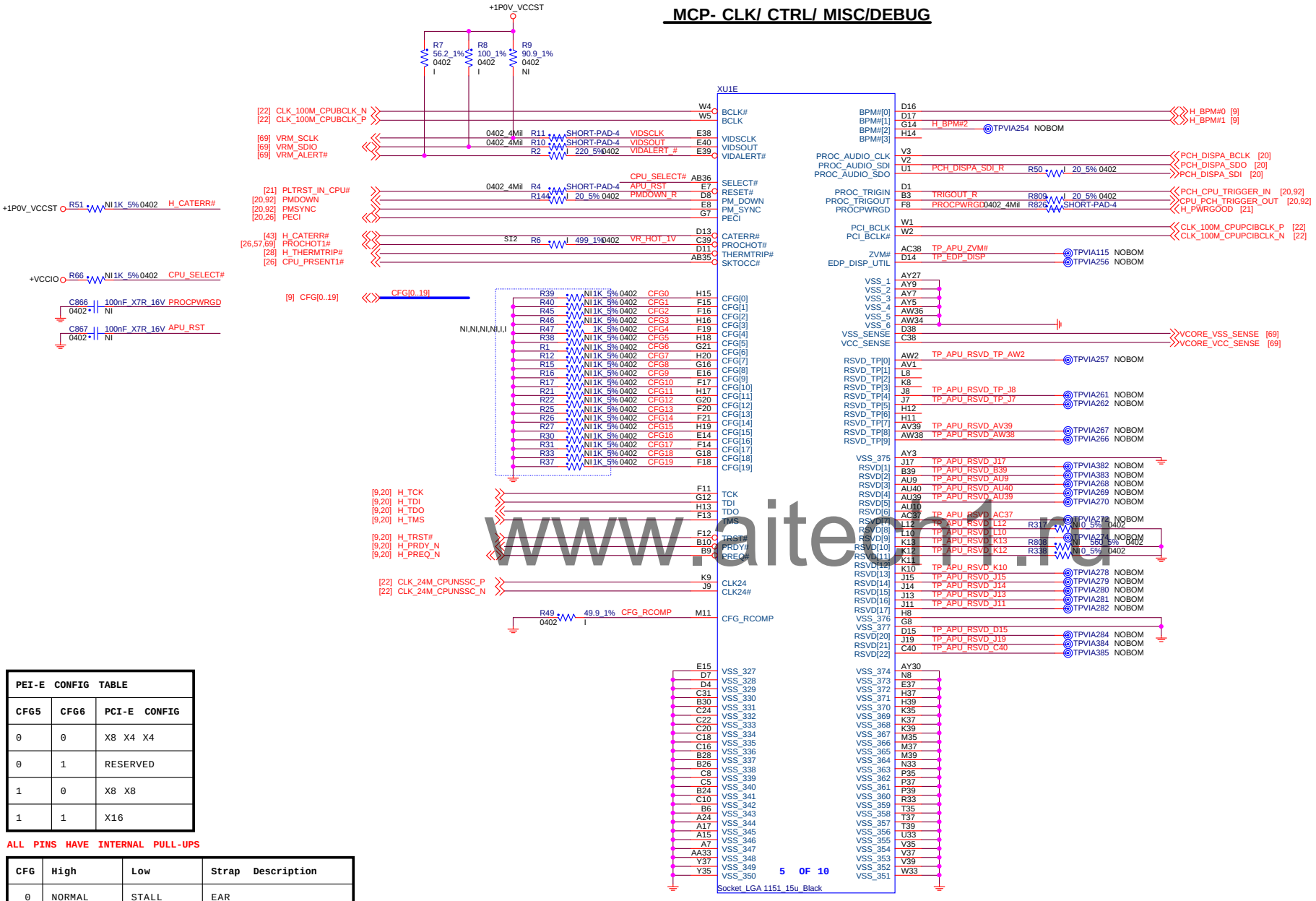
Date: Tuesday, November 15, 2016 | Sheet 9 of 92

MCP- CLK/ CTRL/ MISC/DEBUG



PEI-E CONFIG TABLE		
CFG5	CFG6	PCI-E CONFIG
0	0	X8 X4 X4
0	1	RESERVED
1	0	X8 X8
1	1	X16

ALL PINS HAVE INTERNAL PULL-UPS

CFG	High	Low	Strap Description
0	NORMAL	STALL	EAR
1			RESERVED
2	NORMAL	REVERSE	PEG_LANE_REVERSAL
3			RESERVED
4	DISABLE	ENABLE "0"	eDP enable
5	DISABLE "1"	DISABLE "1"	PEG0CFGSEL[0] x16
6	DISABLE "1"	DISABLE "1"	PEG0CFGSEL[1] x16
7	RESET_N	BIOS REQ	PEG_DEFER_TRAINING
8-19			RESERVED

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

Foxconn Restricted Secret

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Title: MCP- CLK/CTRL/MISC/DEBUG

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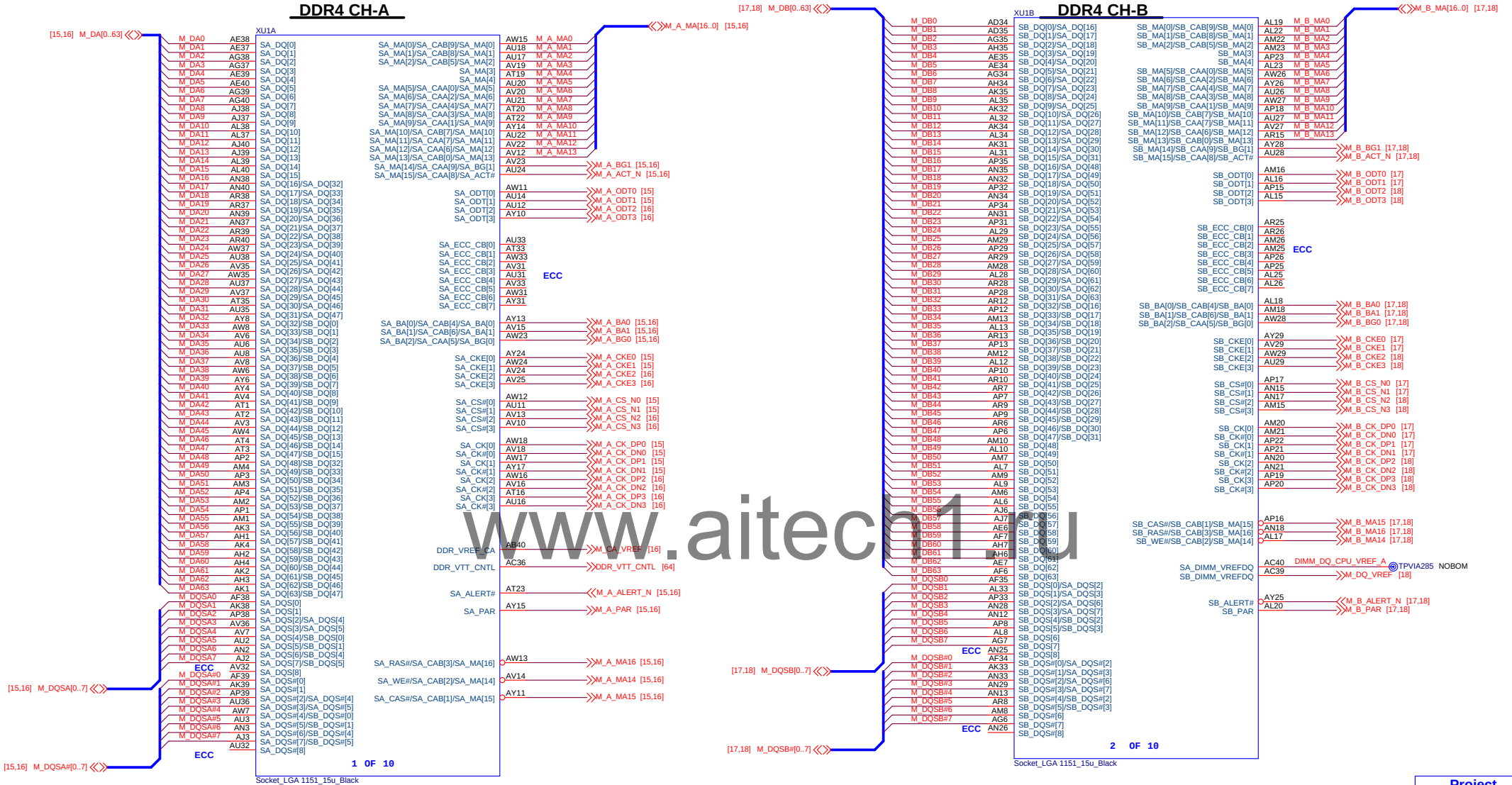
Date: Wednesday, November 09, 2016 | Sheet 10 of 92



Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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Title: MCP- DDR4 CHANNEL A & B

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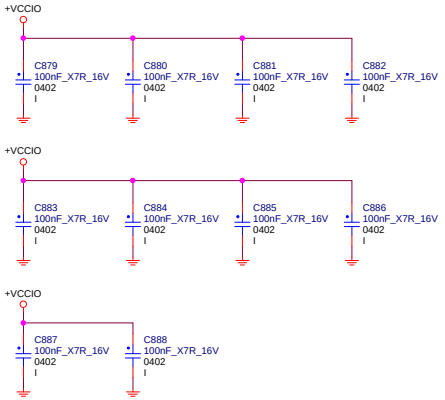
Custom	901015-000	A

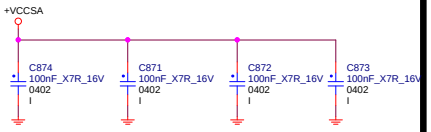
Date: Wednesday, November 09, 2016 Sheet 11 of 92

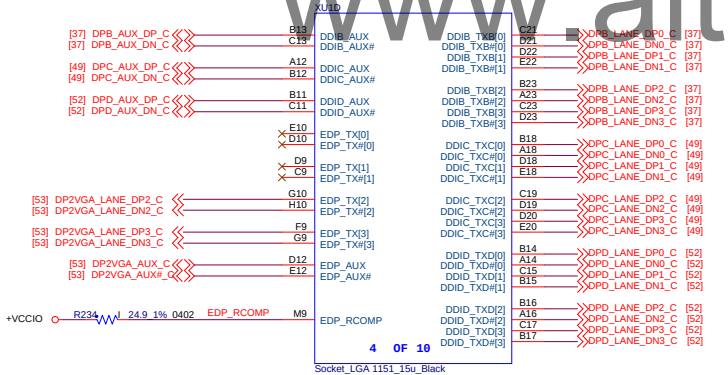
MCP - PEG, DMI, DDI

STICHING CAP for PEGx16 Note 1



STItCHING CAP for DMI Note 1





Design Note

Note 1

Place Stitching Capfor PEGx16 @crossing- moat area

Place Stitching Capfor DMI @crossing- moat area

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

Foxconn Restricted Secret

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Title: MCP- PCI/DMI/DDI

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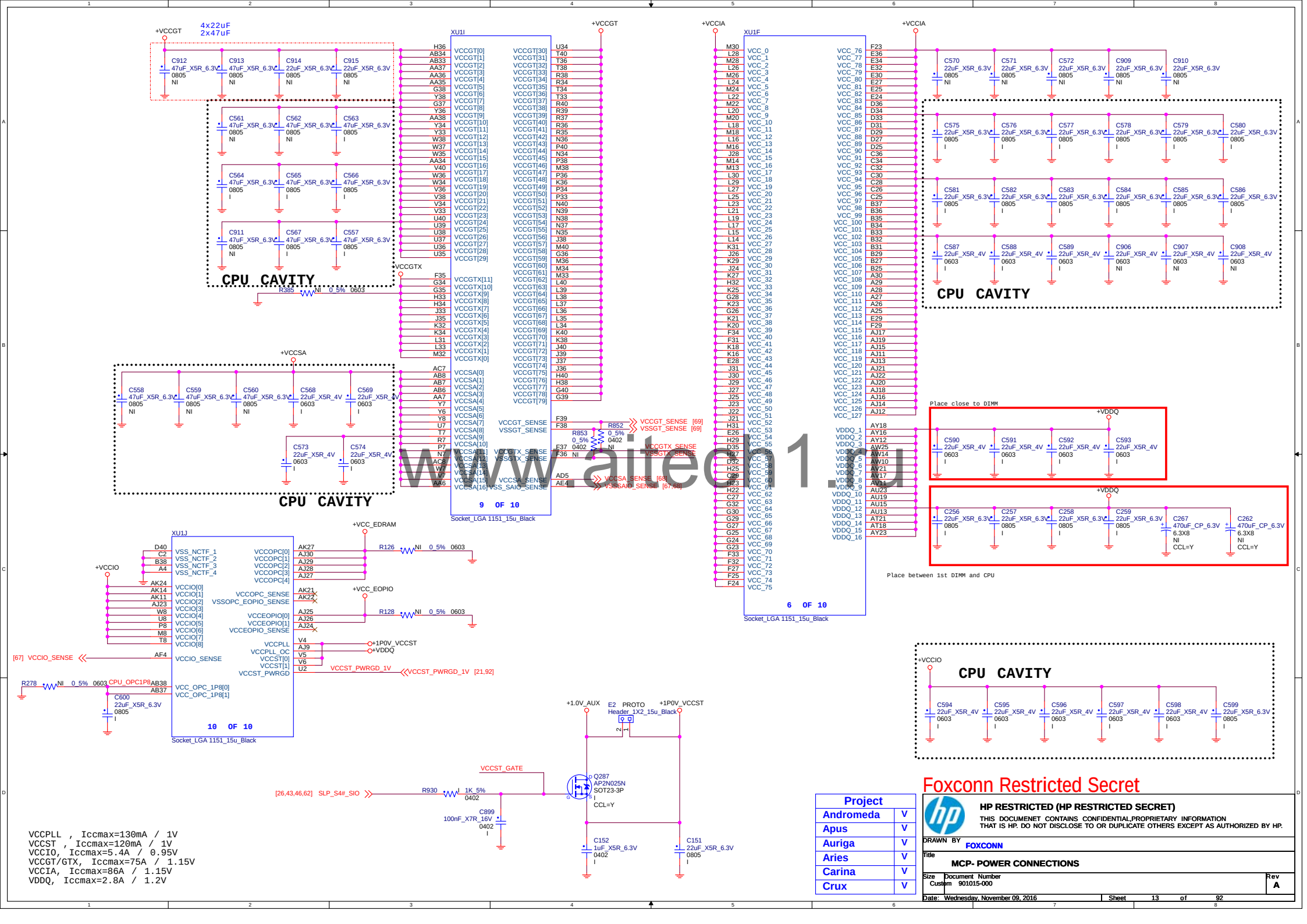
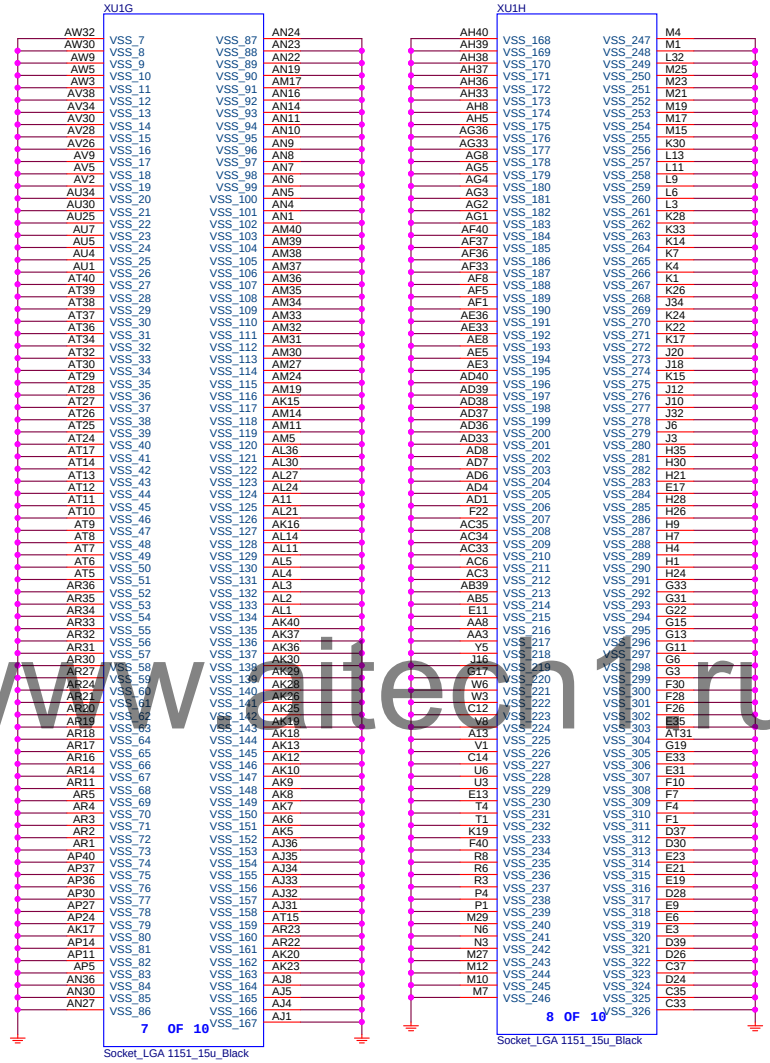
Date: Wednesday, November 09, 2016 | Sheet 12 of 92





Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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Title MCP- VSS

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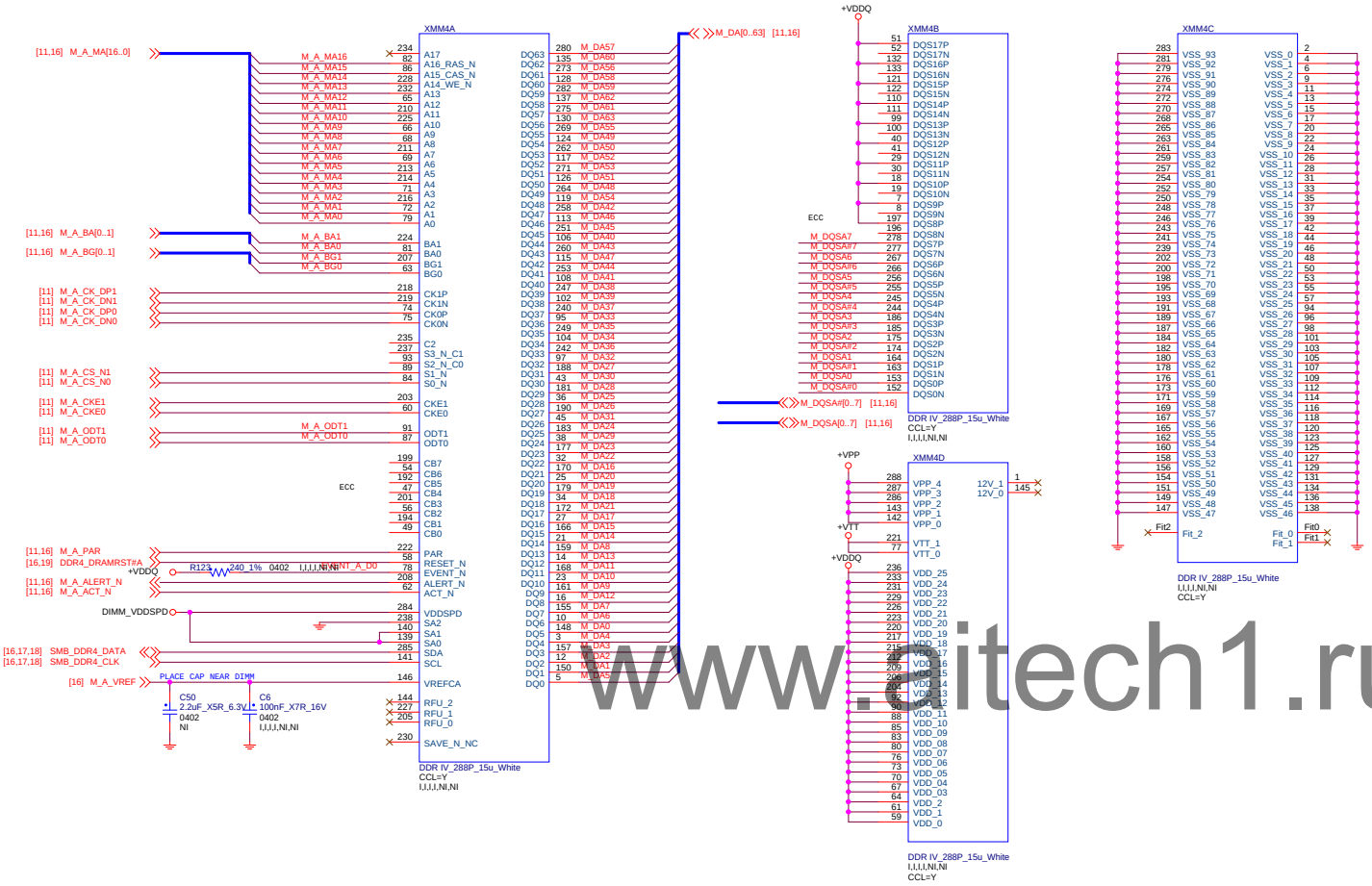
Date: Wednesday, November 09, 2016 | Sheet 14 of 92

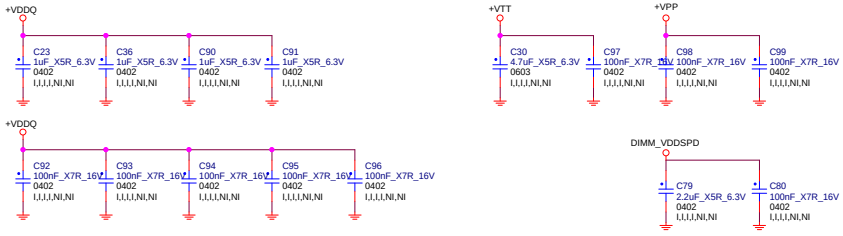
DDR4 CHA D0 XIMM4

Note 1 Note 2

CHA-D0-XMM4



Decoupling CAP



Design Note

Note 1

SPD ADDRESS: 011

SMBUS ADDRESS: A6

Note 2

BOM DISTRIBUTION RULE

Andromeda, Apus, Auriga, Aries, Carina, Crux (BOM,BOM,BOM,BOM,BOM,BOM)

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	X
Crux	X

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Title: DDR4 CHA D0 XIMM4

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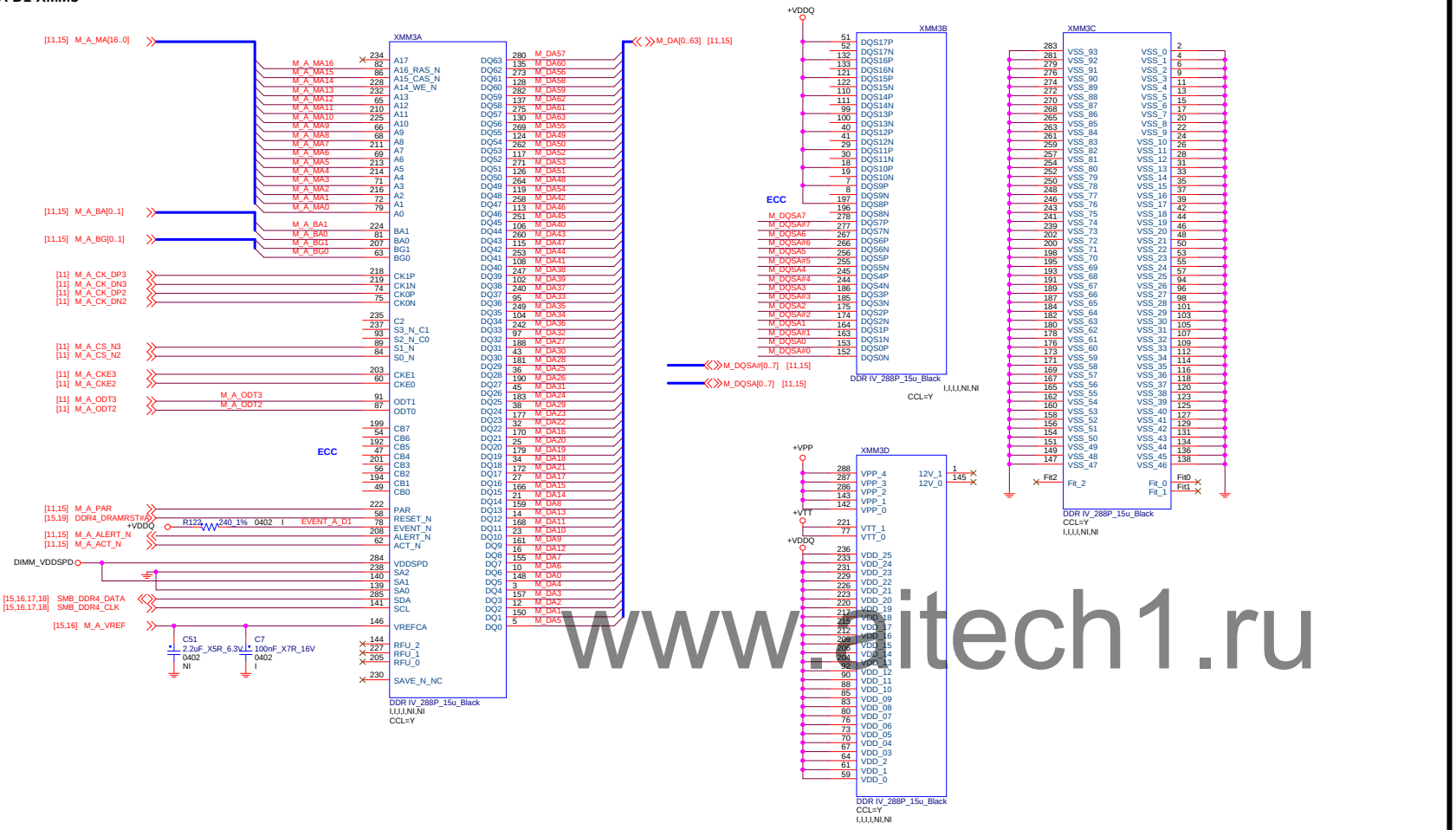
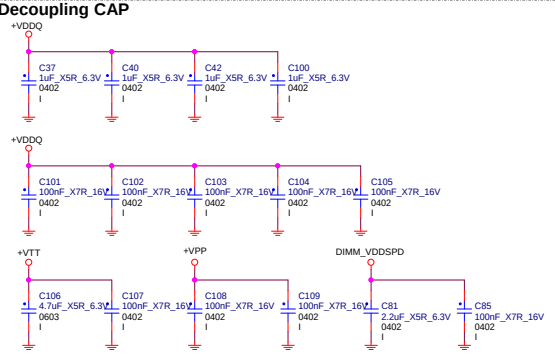
Date: Wednesday, November 09, 2016 Sheet 15 of 92

DDR4 CHA D1 XIMM3 Note1 Note 3

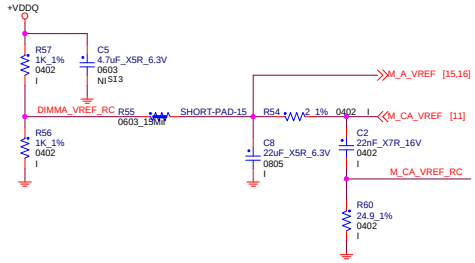
CHA-D1-XMM3



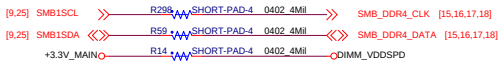
Decoupling CAP



CH-A VREFCA

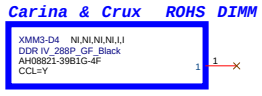


SMBUS/SPD PWR



D4 DIMM Slot - CHA

Note 2



Design Note

Note 1

SPD ADDRESS: 010

SMBUS ADDRESS: A4

Note 2

XMM3-D4 only for D4 porjects

Note 3

BOM DISTRIBUTION RULE

Andromeda, Apus, Auriga, Aries, Carina, Crux (BOM,BOM,BOM,BOM,BOM,BOM)

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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Title: DDR4 CHA D1 XIMM3

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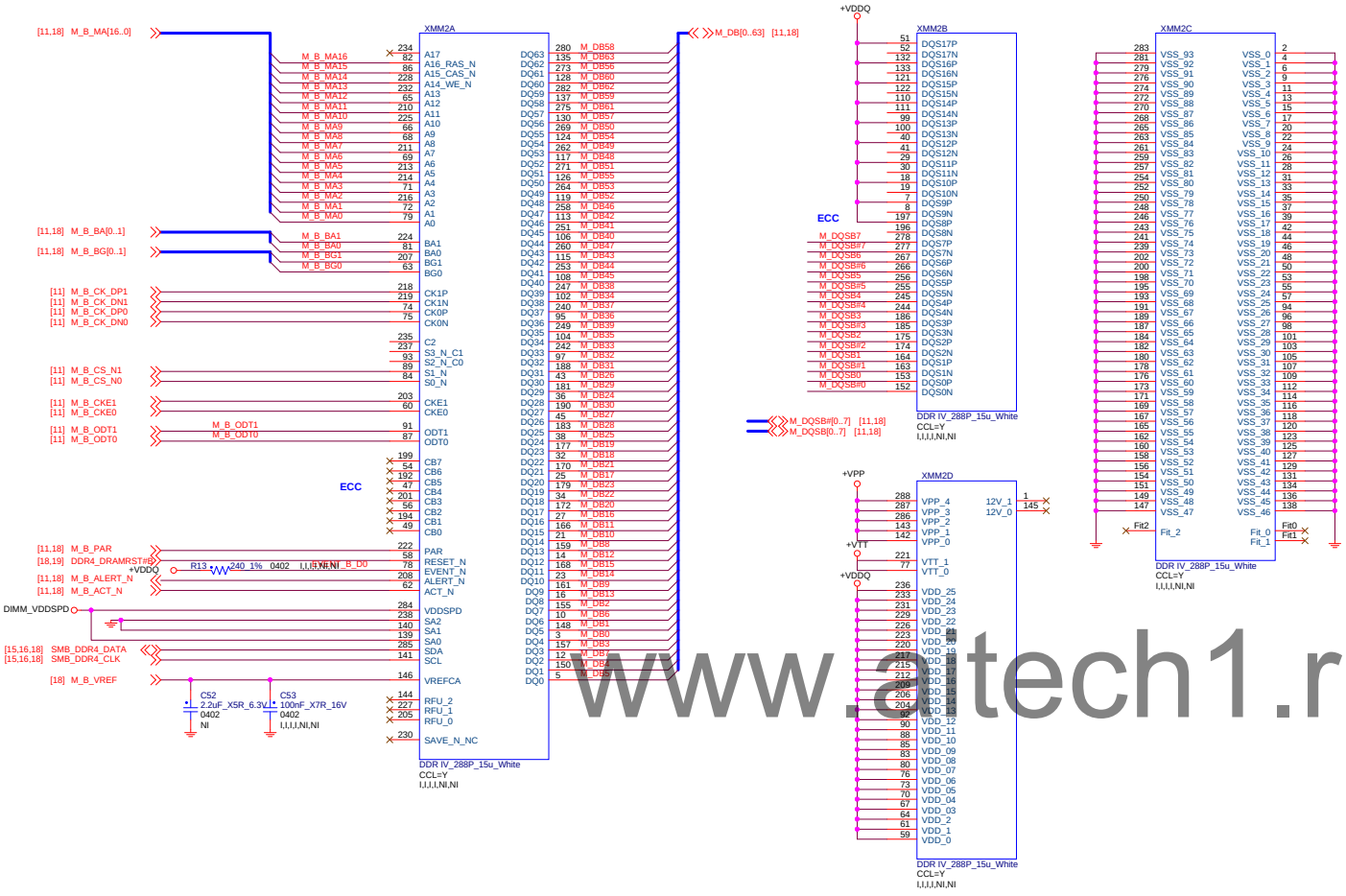
C	901015-000	A

Date: Wednesday, November 09, 2016 Sheet 16 of 92

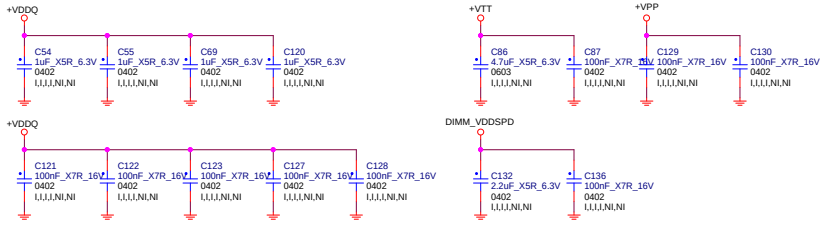
DDR4 CHB D0 XIMM2

Note 1 Note 2

CHB-D0-XMM2



Decoupling CAP



Design Note

Note 1

SPD ADDRESS: 001

SMBUS ADDRESS: A2

Note 2

BOM DISTRIBUTION RULE

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Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	X
Crux	X

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Title: DDR4 CHB D0 XIMM2

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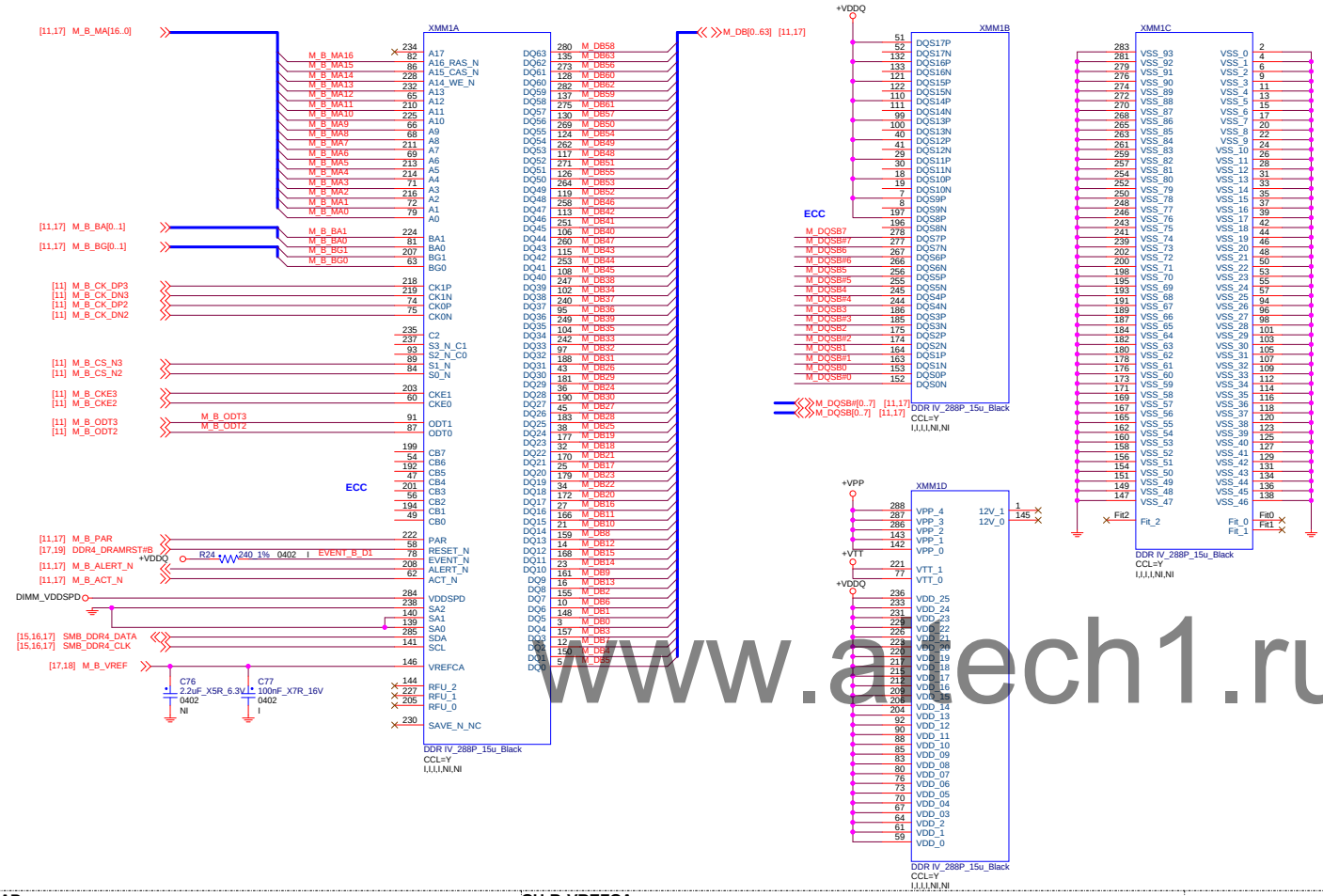
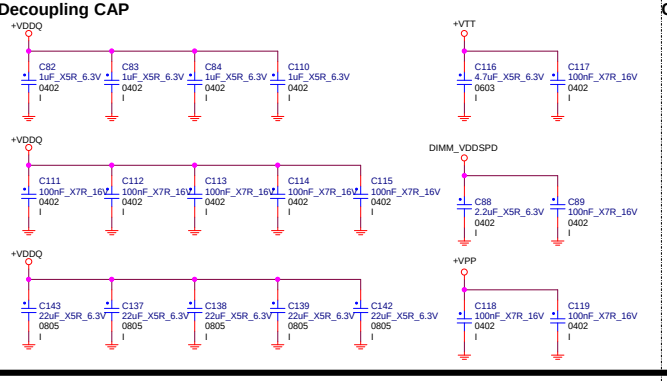
Date: Wednesday, November 09, 2016 Sheet 17 of 92

DDR4 CHB D1 XIMM1 Note 1 Note 3

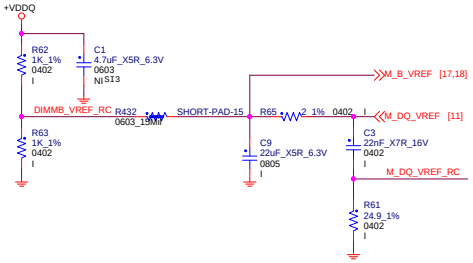
CHB-D1-XMM1



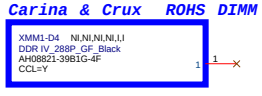
Decoupling CAP



CH-B VREFCA



Carina & Crux ROHS DIMM



Design Note

Note 1

SPD ADDRESS: 000

SMBUS ADDRESS: A0

Note 2

XMM1-D4 only for D4 porjects

Note 3

BOM DISTRIBUTION RULE

Andromeda, Apus, Auriga, Aries, Carina, Crux (BOM,BOM,BOM,BOM,BOM,BOM)

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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Title DDR4 CHB D1 XIMM1

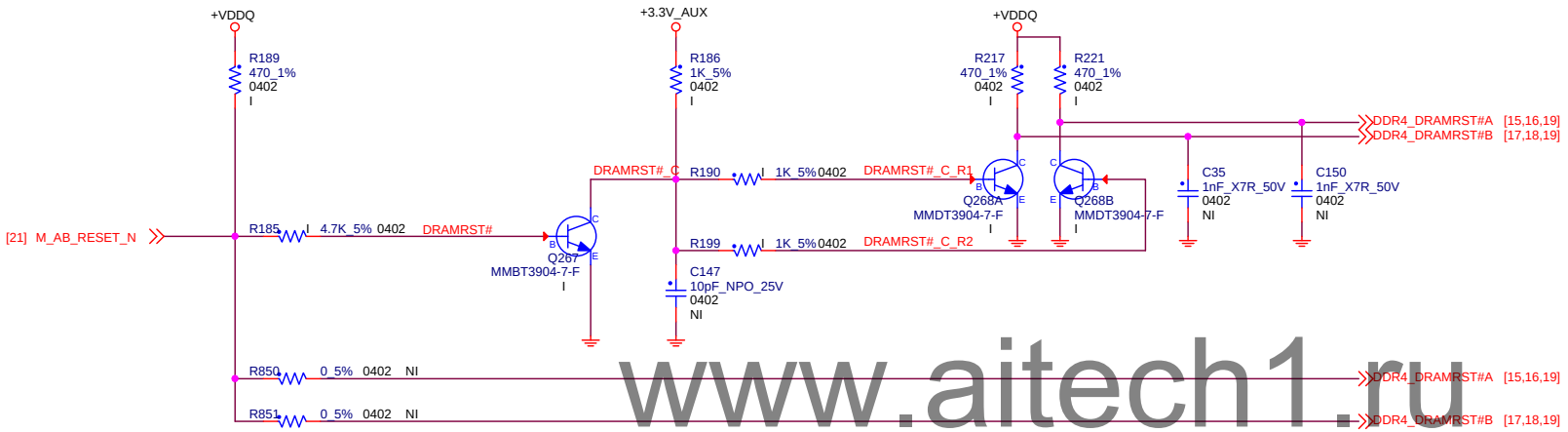
Size	Document Number	Rev
C	901015-000	A

Date: Wednesday, November 09, 2016 Sheet 18 of 92

DDR RESET

DDR4 DRAMRST# BUFFER CIRCUIT

Note 1



Design Note

Note 1
Place these circuit close to DIMM

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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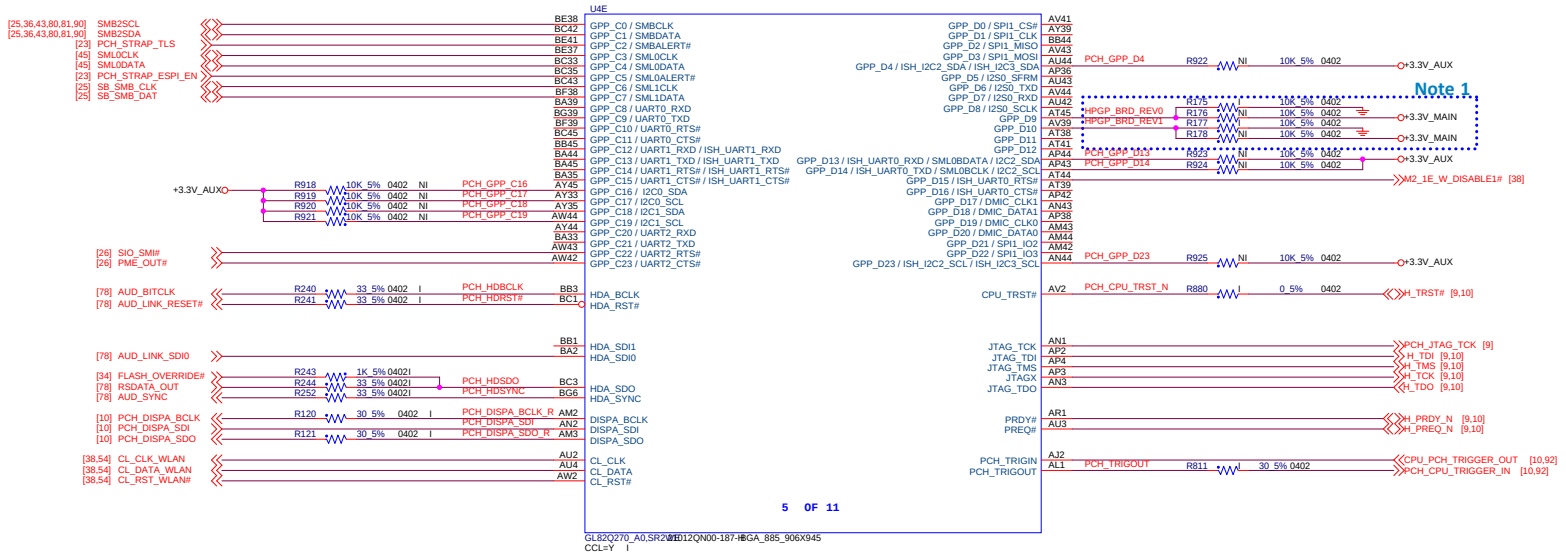
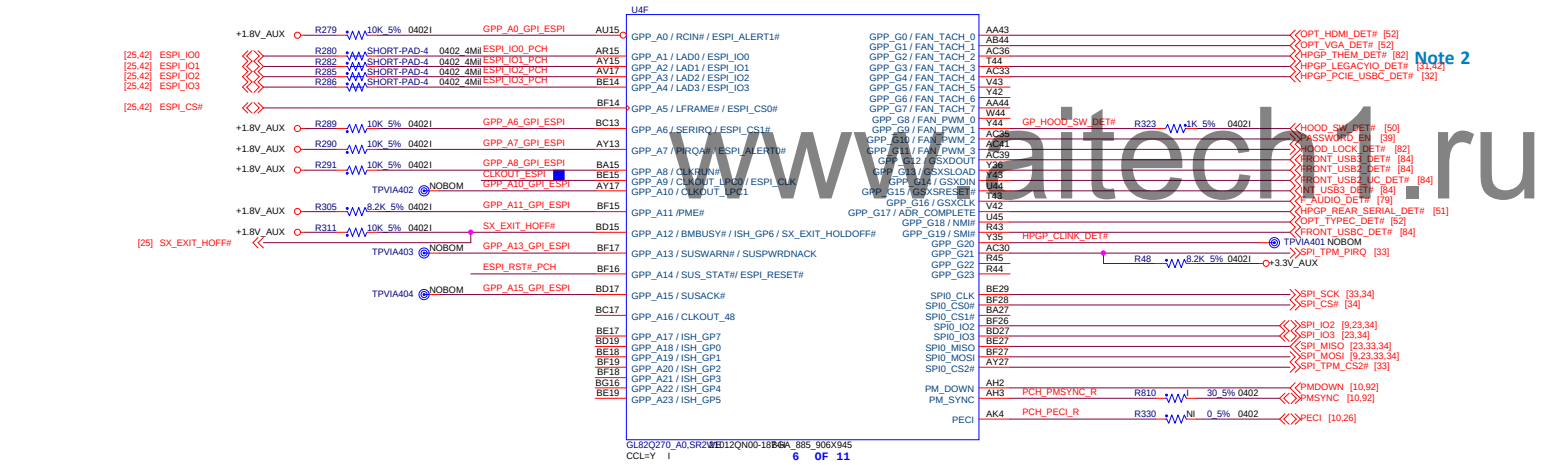
Title: DDR_RESET

Size	Document Number	Rev
B	901015-000	A

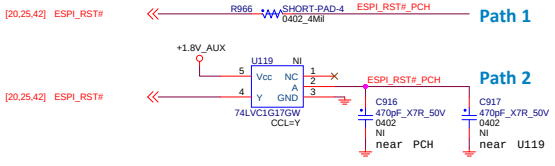
Date: Wednesday, November 09, 2016 Sheet 19 of 92

PCH - (E)SPI/HDA/SMB/GPIO





ESPI RESET# Path



ESPI CLOCK Path

Design Note

Note 1
Board Revision ID [1:0]

	BRD_REV1 GPP_D10		BRD_REV0 GPP_D9	
	R178(pull high)	R177 (pull down)	R176 (pull high)	R175(pull down
DB 00	NI	I	NI	I
SI 01	NI	I	I	NI
PV 10	I	NI	NI	I
PVT2+ 11	I	NI	I	NI
MVB,A 00	NI	I	NI	I
1st major ECN 01	NI	I	I	NI
2nd major ECN 10	I	NI	NI	I
3rd major ECN 11	I	NI	I	NI

Note 2

HPGP_THEM_DET# Change to TP only in Page88. D8 TWR do not support Cabled Ambient Sensor. SIO1287654

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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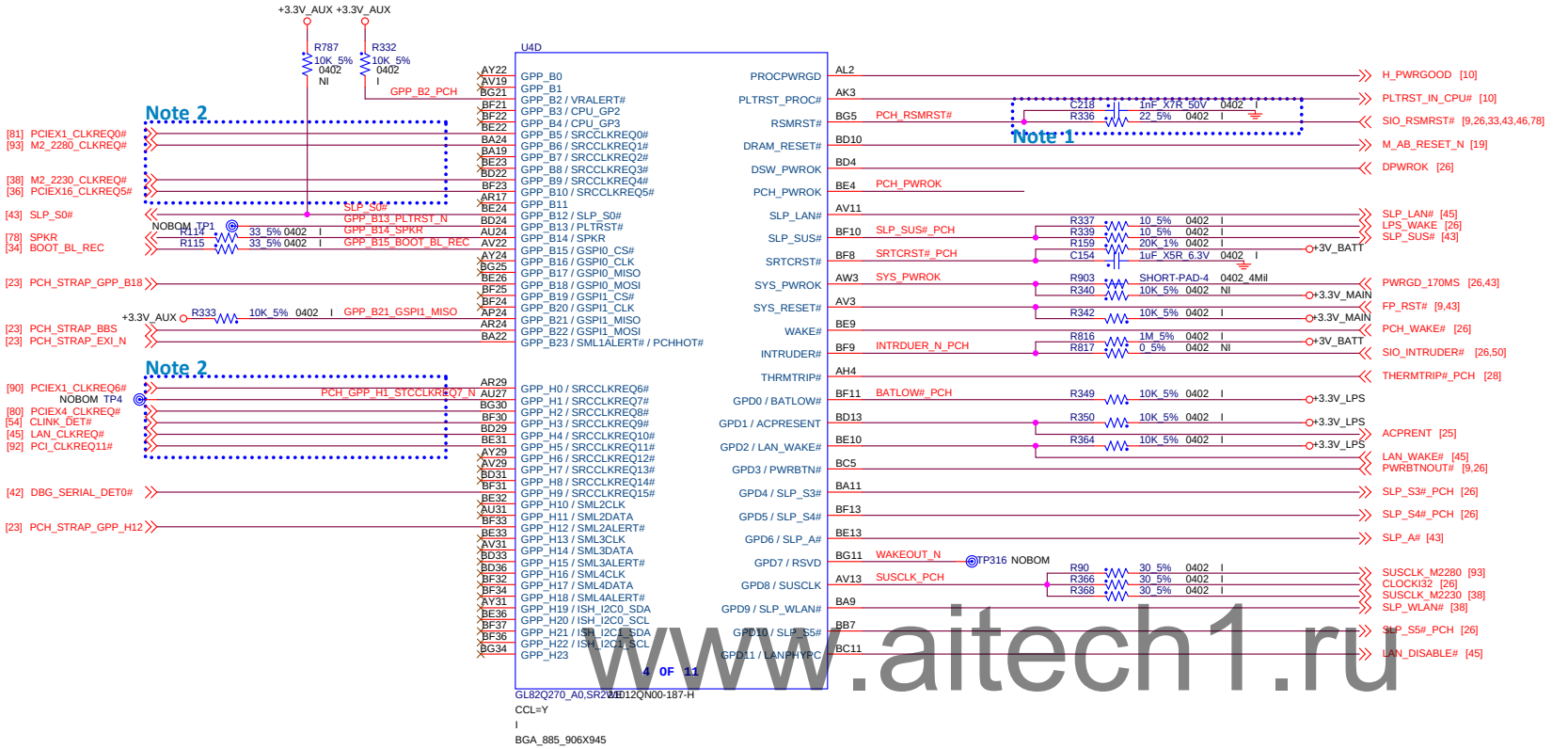
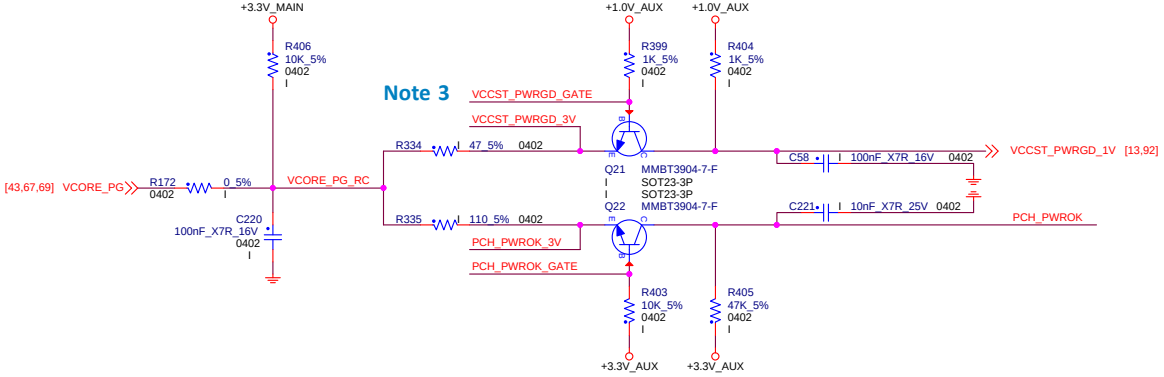
Title: PCH - (E)SPI/HDA/SMB/GPIO

Size	Document Number	Rev
C	901015-000	A

Date: Wednesday, November 09, 2016 | Sheet 20 of 92

PCH - GPIO/MISC





Design Note

Note 1

Place R901 close to PCH
Place C219 close to PCH
Place C218 close to PCH
Place R336 close to Tpoint

Note 2

SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements

SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs

SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs

Note 3

C58 place to CPU area as closed as possible

C221 place to PCH area as closed as possible

R335, R403, R405, R406, Q22 Place together and close to PCH

R334, R339, Q21, R401 Place together. Avoid colse to Vcore Vin and other PWR Phase

R172 and C220 Place close to Vocre Controller (PU100)

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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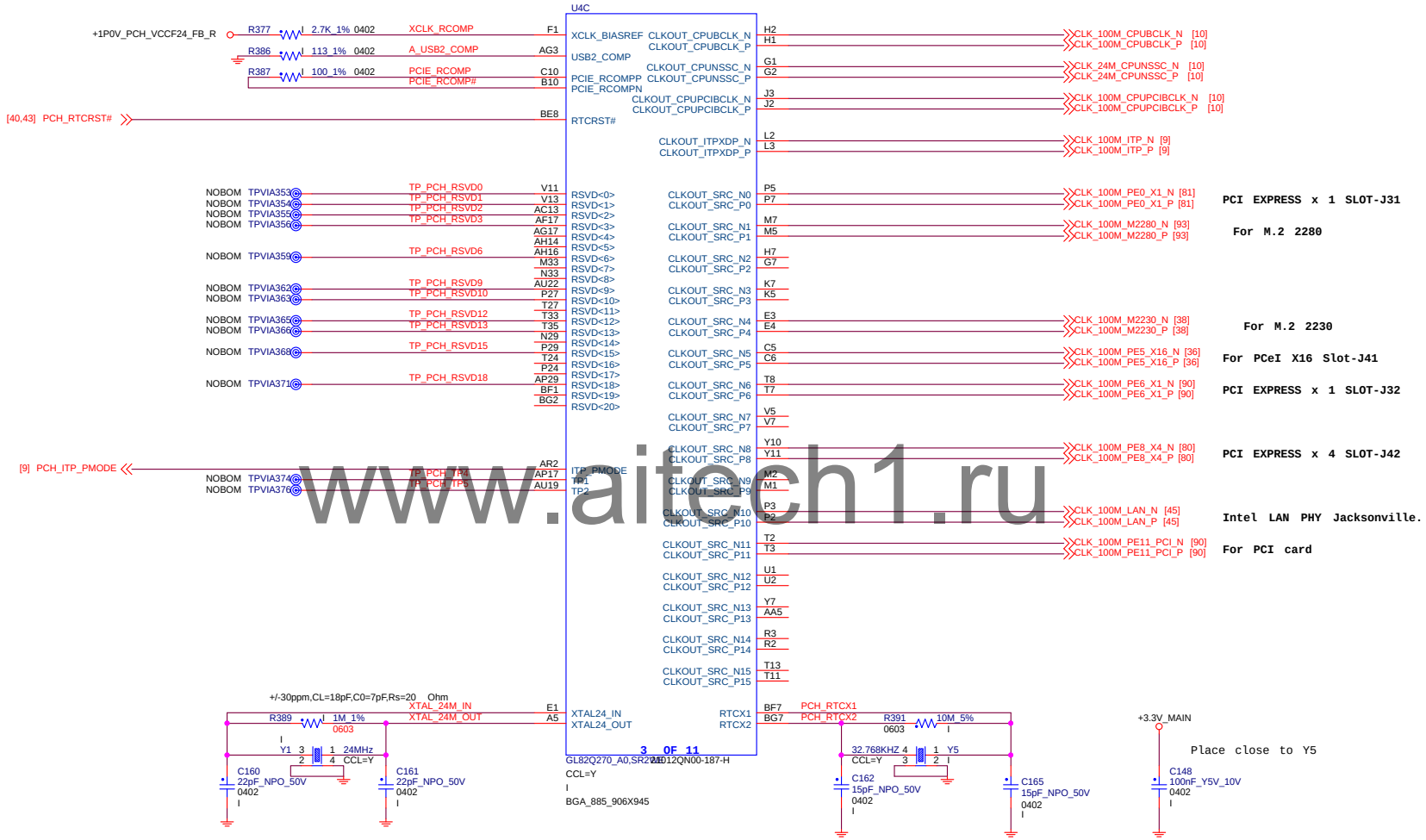
Title PCH - GPIO/MISC

Size Custom | Document Number 901015-000 | Rev A

Date: Wednesday, November 09, 2016 | Sheet 21 of 92

PCH - CLOCK DISTRIBUTION



Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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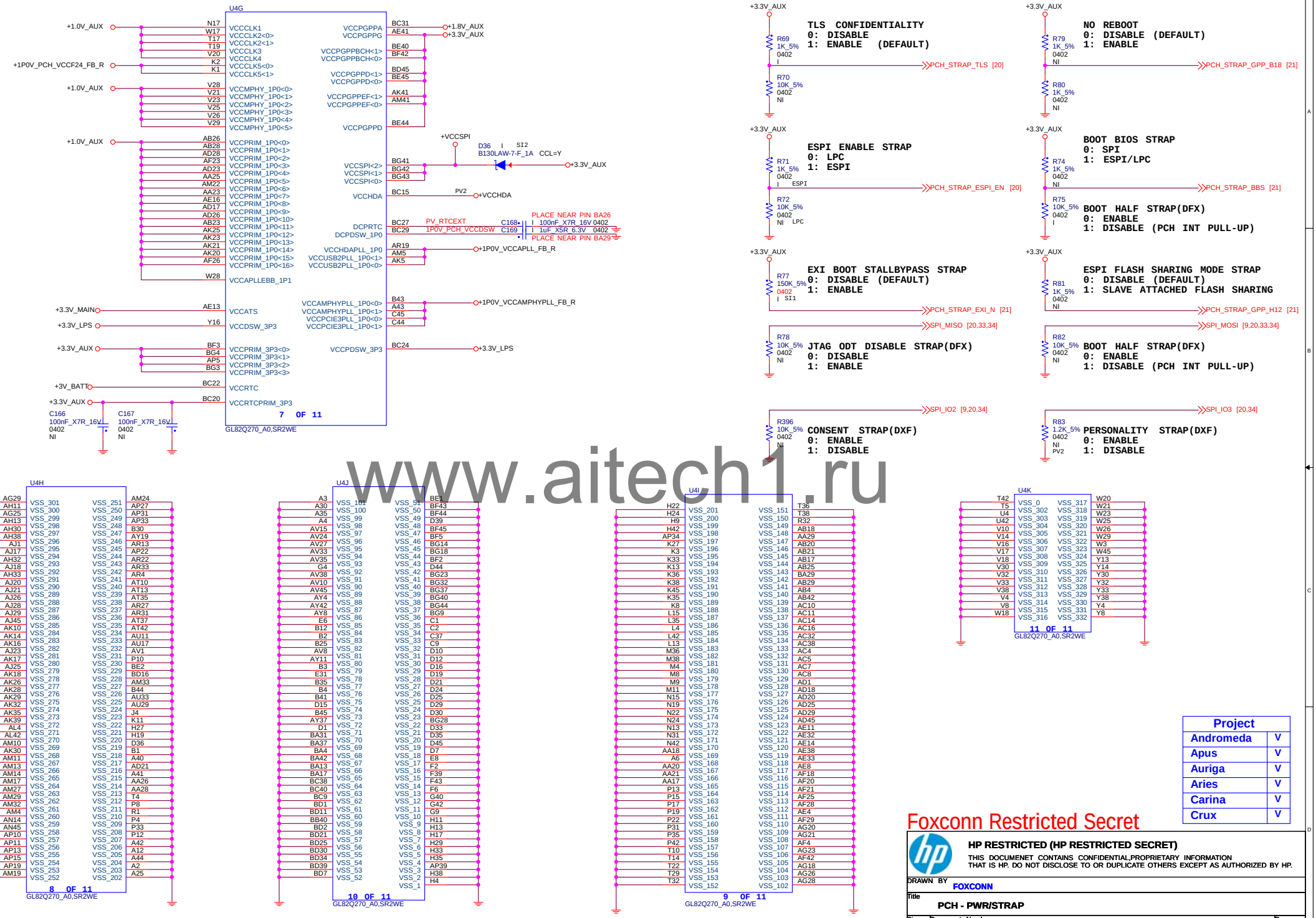
Title: PCH - CLOCK

Size: Custom | Document Number: 901015-000 | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 22 of 92



Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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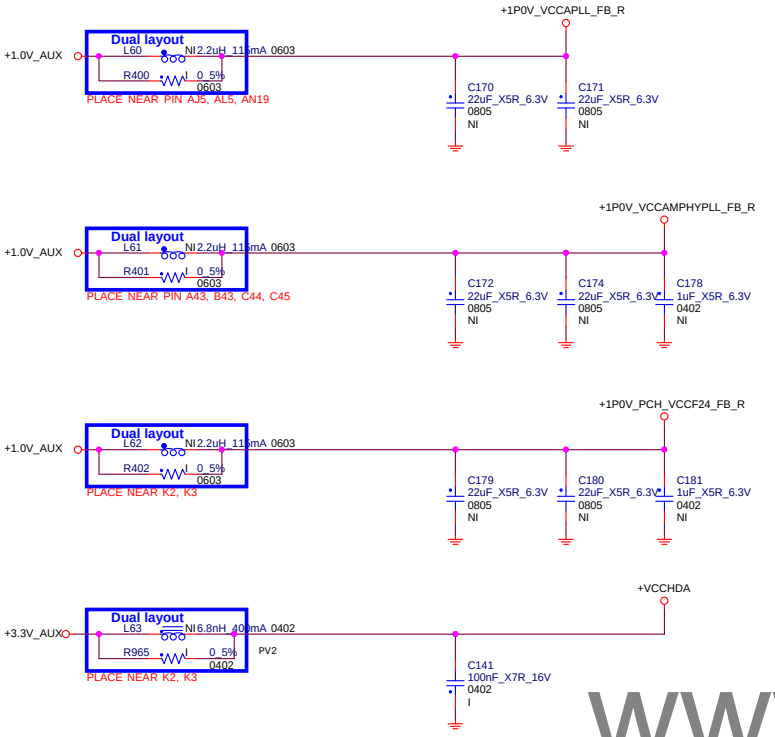
Title PCH - PWR/STRAP

Size Custom | Document Number 901015-000 | Rev A

Date: Wednesday, November 09, 2016 | Sheet 23 of 92

FILTER

SKYLAKE Decoupling & filter

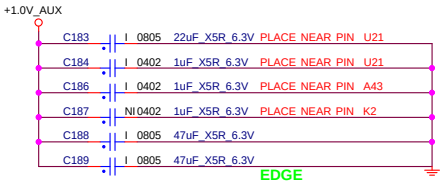


Power Plane Isolation

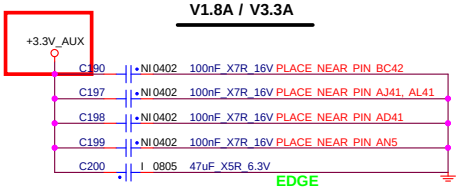
Need to update for SLK

Voltage	Interface	PCH Pins sharing power rail
VCC_PCH 1.05V	Core	U26, U25, U23, U21, V26,
	PCIe/SATA/ USB3	T19, T20, P22, P23, P25, P26, P28, P14, P16, P17
	GPIO/LPC	AC12
	FDI	M14
	DIFFCLK	U12, V14
		W14
		AB2
	SSC	T16, V16
		AA16, W16
	USB2	AF19, AF20, AF22, AF23, AP22
PCH 3.3V Standby	SUS	AM33, AN33
	USB2	AH18, AH20, AH22, AJ20, AK20
	AZALIA	AW26
	USB3	P20
	RTC	AP35
PCH 3.3V	CLK	AM7, AM9, AP5, AP7, AR4, AT5, AV4, AW4, AW9, AG12, AK11,
	HVCMOS	AG1
	PCIe	AV3, AW3
	Core	U30, W30
	Fuse	AF26

V1.0A

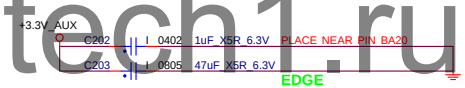


V1.8A / V3.3A

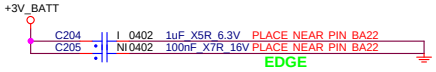


V1.8A / V1.8S / V3.3S

V3.3A

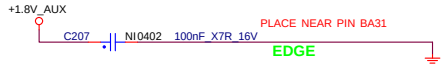


VCCRTC



V3.3 DSW

VccPGPPA



Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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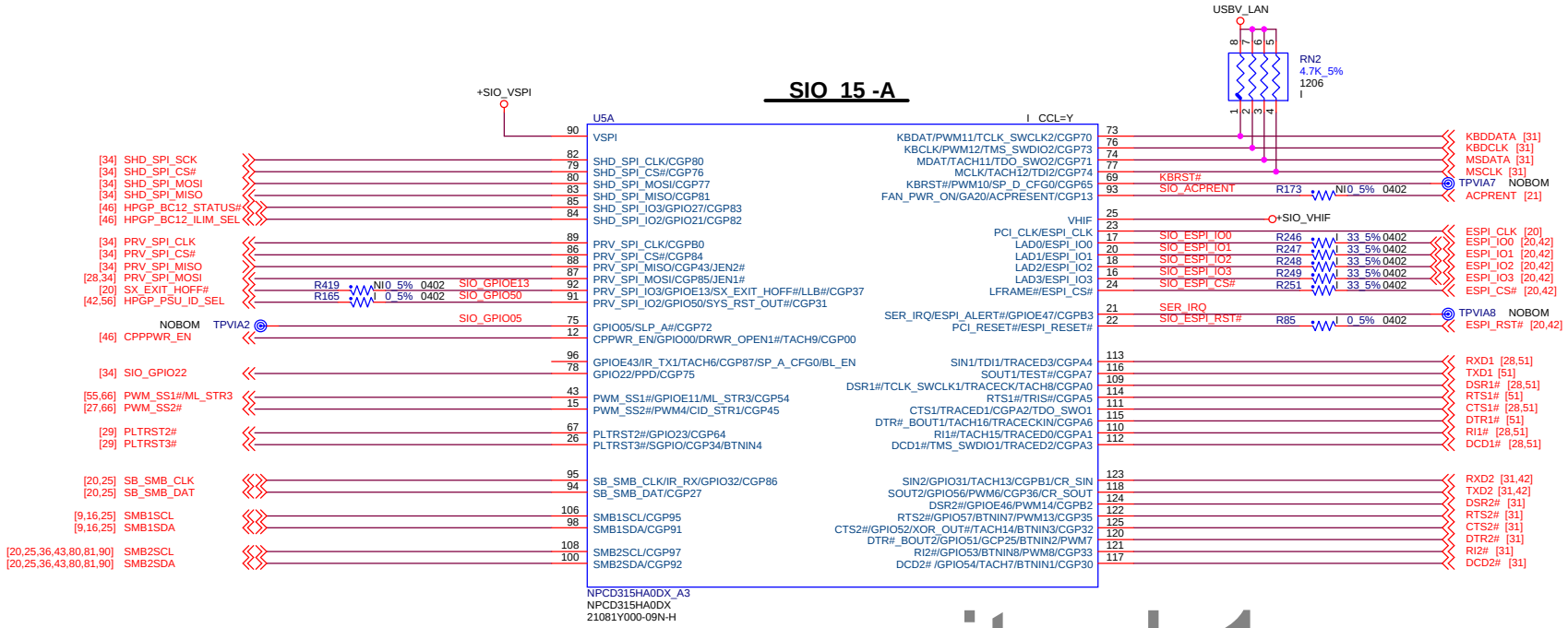
Title: PCH-PLL FILTER & DECOUPLING

Size: Custom | Document Number: 901015-000 | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 24 of 92

SIO1

SIO_15 -A

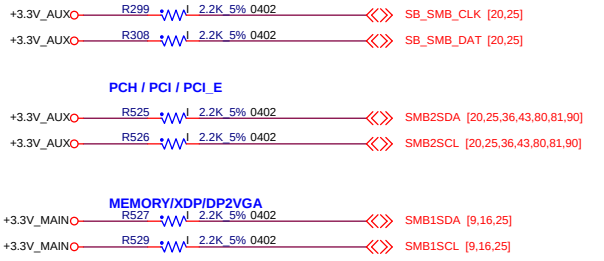


Design Note

Note 1

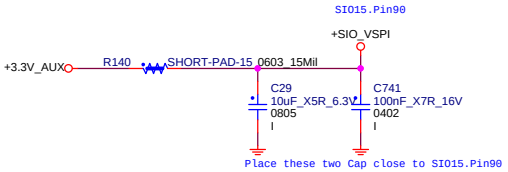
Place these two Cap close to SIO15.Pin90

SMBUS PU

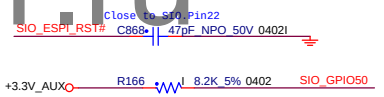


SIO SPI Power

Note 1



SIO HW Config



Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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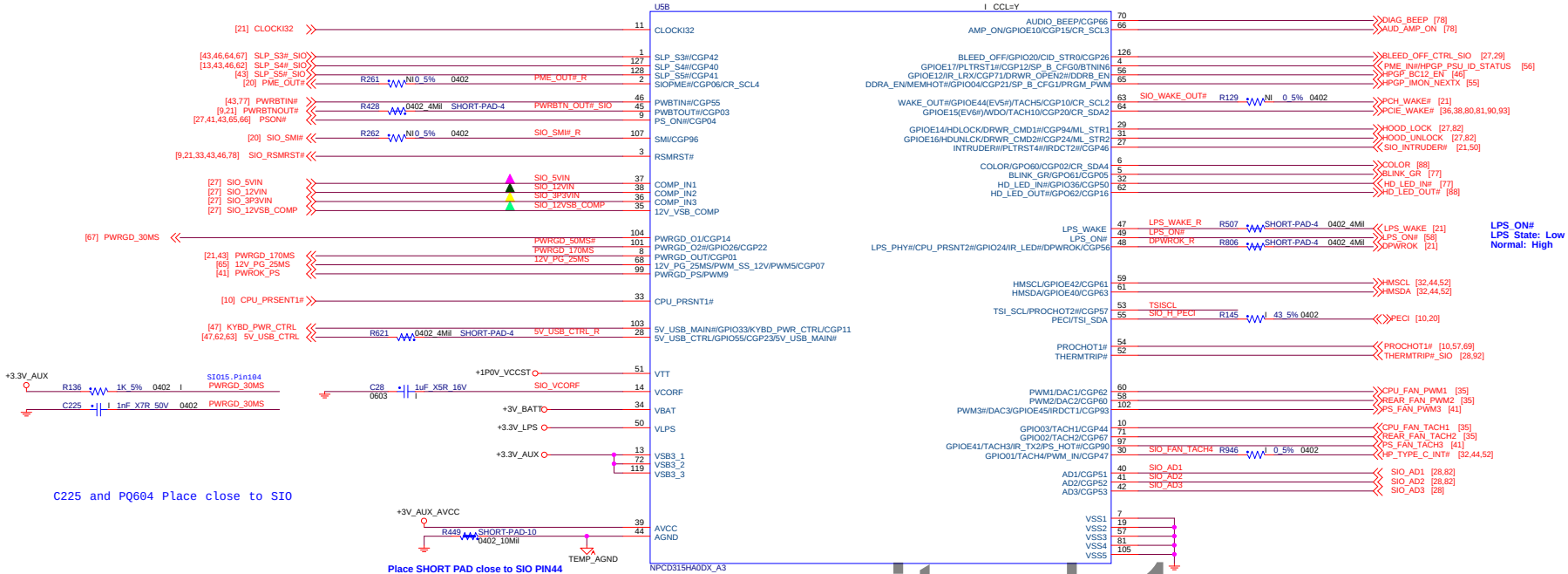
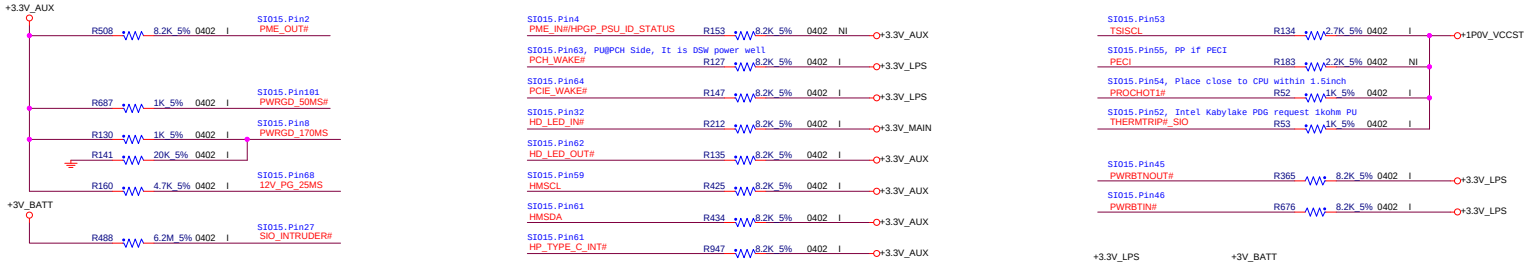
Title: SIO_1

Size: Custom | Document Number: 901015-000 | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 25 of 92

SIO5-B





Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

Foxconn Restricted Secret

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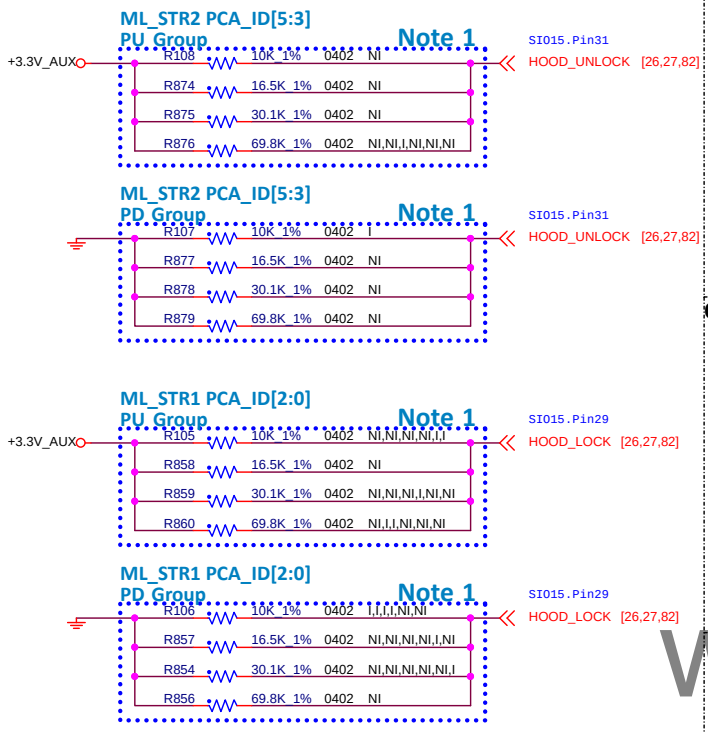
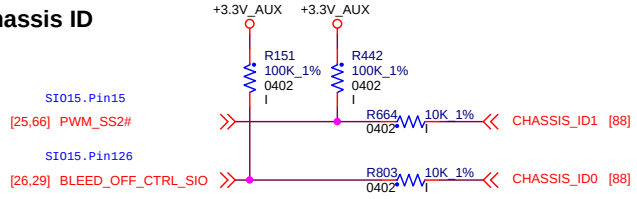
Title	SIO_2	
Size C	Document Number 901015-000	Rev A
Date: Wednesday, November 09, 2016	Sheet 26 of 92	

SIO_3

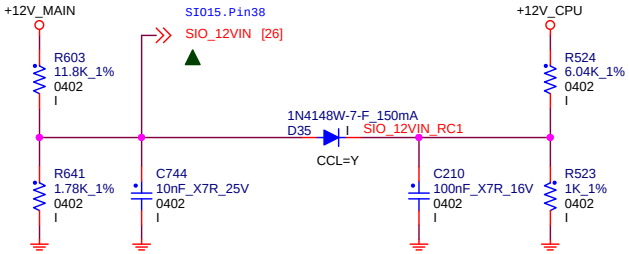
PCA Board ID



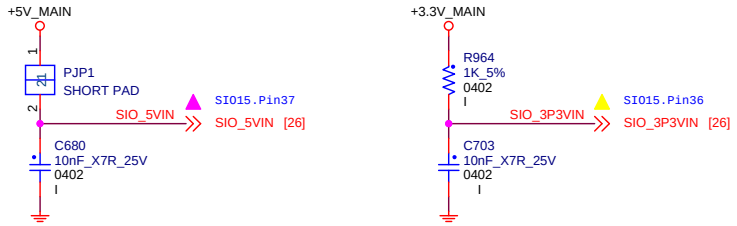
Chassis ID



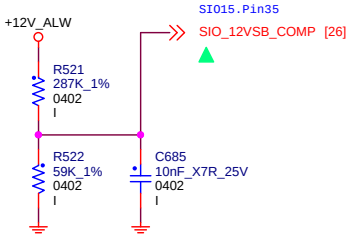
12V_VSB_COMP - ENT17
+12V_CPU Monitor - ENT17



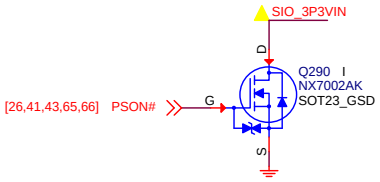
COMP1/3



COMP2_+12V - ENT17



COMP3
Sure Start Discharge



Design Note

Note 1

R108/R876/R875/R874 co-lay
R107/R879/R878/R877 co-lay
R105/R858/R859/R860 co-lay
R106/R854/R856/R857 co-lay
PCA_ID Resistor values

		ML_STR2 pin		ML_STR1 pin	
PCA	PCA_ID	R108 PU 1%	R107 PD 1%	R105 PU 1%	R106 PD 1%
Andromeda	00h	NI	10K	NI	10K
Apus	01h	NI	10K	69.8K	10K
Aries	02h	NI	10K	30.1K	10K
Auriga	11h	69.8K	10K	69.8K	10K
	04h	NI	10K	16.5K	16.5K
Carina	05h	NI	10K	10K	16.5K
Crux	06h	NI	10K	10K	30.1K
	7	NI	10K	10K	69.8K

Andromeda, Apus, Auriga, Aries, Carina, Crux (BOM,BOM,BOM,BOM,BOM,BOM)

Change CROWBARD circuit follow HP request. R603 PWR change to +12V_MAIN and its devider circuit connect to SIO_12VIN. R521 PWR change to +12V_ALW and its devider circuit connect to SIO_12VSB_COMP. SIO1296502

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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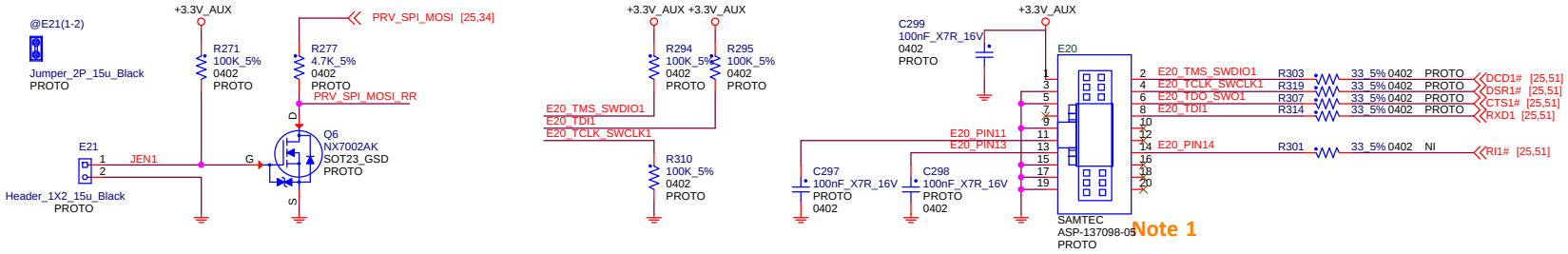
Size B | Document Number 901015-000 | Rev A
Date: Wednesday, November 09, 2016 | Sheet 27 of 92

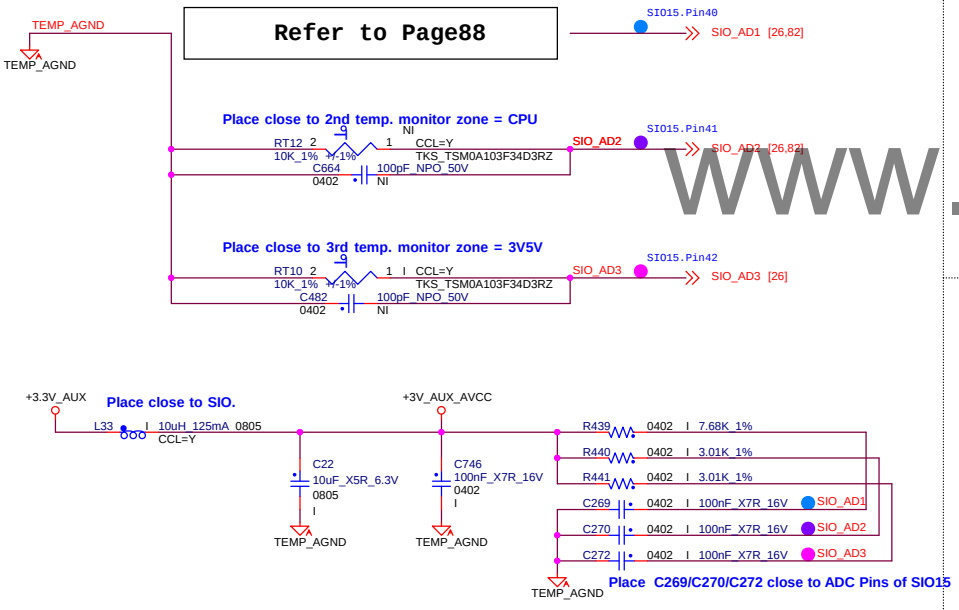
SIO4

SIO15 DEBUG HEADER

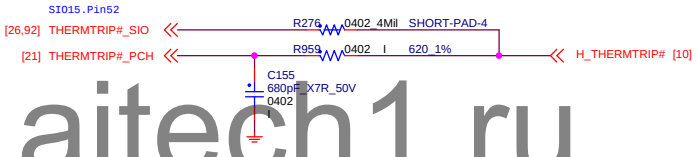


Note 1

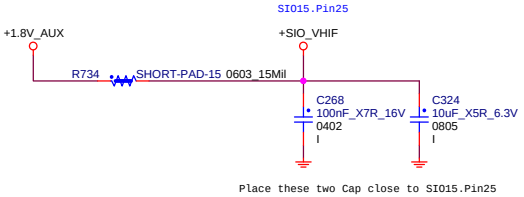
THERMAL SENSORs (SIO15)



THERMTRIP#



SIO eSPI Power



Design Note

Note 1: E20 Footprint

NPI
HDT_2X10_50

MVB
HDT_2X10_50_MVB

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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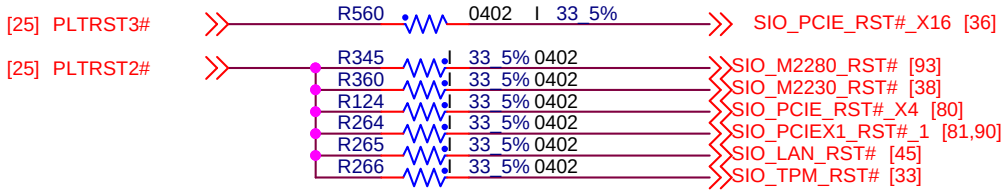
Title: SIO_4

Size: Custom | Document Number: 901015-000 | Rev: A

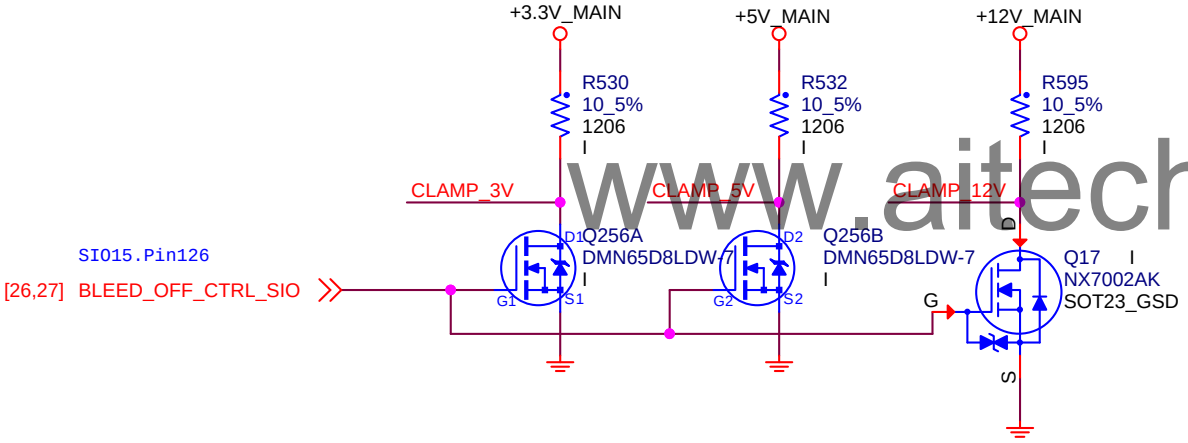
Date: Wednesday, November 09, 2016 | Sheet 28 of 92

SIO5

PCIE_RST



BLEED OFF 3.3V / 5V /12V



Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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Title: SIO_5

Size	Document Number	Rev
A	901015-000	A

Date: Wednesday, November 09, 2016 | Sheet 29 of 92

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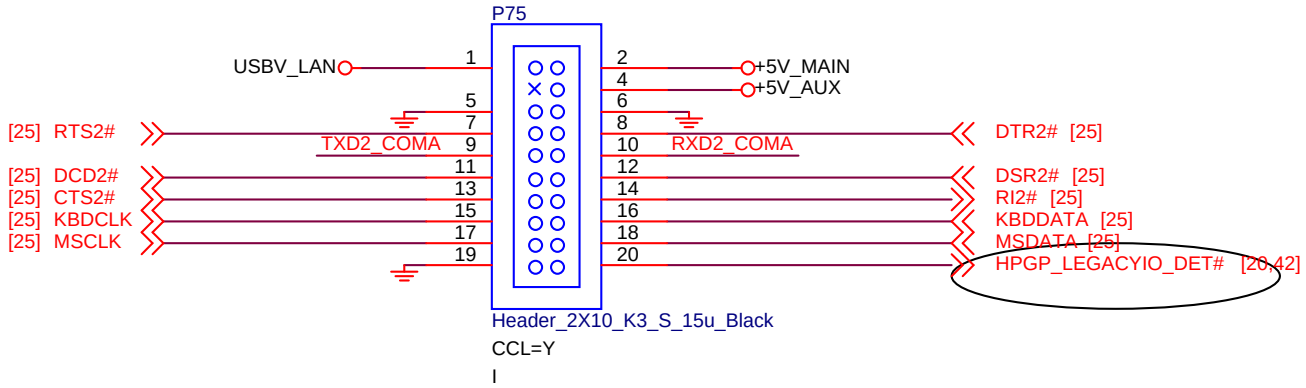
Size	Document Number	Rev
B	901015-000	A

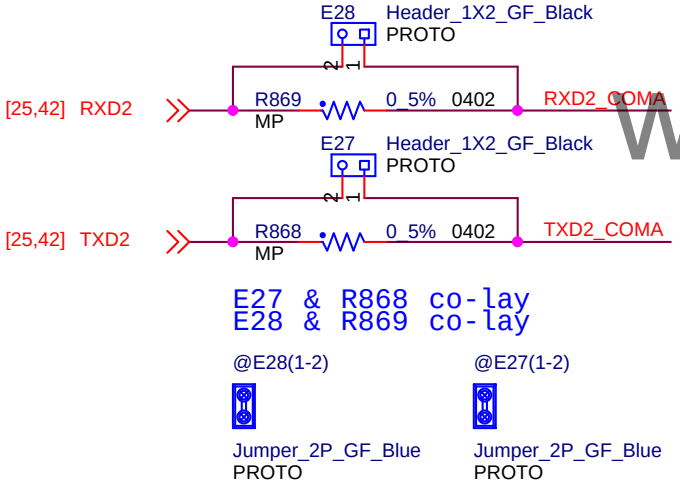
Date: Wednesday, November 09, 2016 Sheet 30 of 92

LEGACY-IO

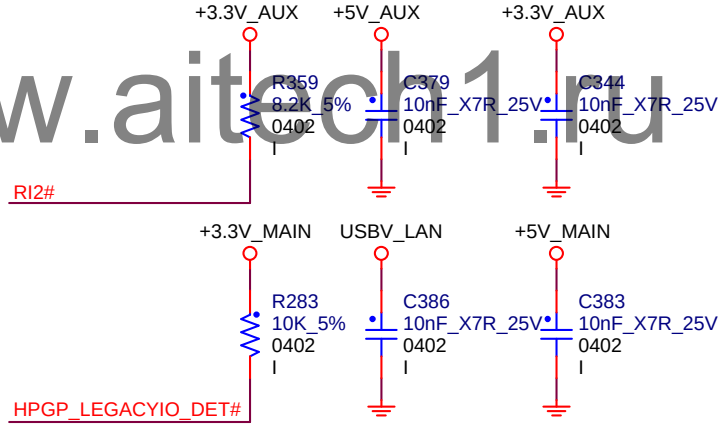
Serial Port + PS2 Header



2nd Serial Port + PS2 Debug



2nd Serial Port + PS2 Decoupling Cap and Pull-Up



Design Note

Note 1
PINOUT

P74 - ENT17

2nd Serial + PS2

1 +5V_USB	2 +5V_MAIN
3 KEY	4 +5V_VSB
5 GND	6 GND
7 RTS#	8 DTR#
9 TXDAT	10 RXDAT
11 DCD#	12 DSR#
13 CTS#	14 RI#
15 GND	16 KBDAT
17 KBCLK	18 MSDAT
19 MSCLK	20 DETECT GPIO#

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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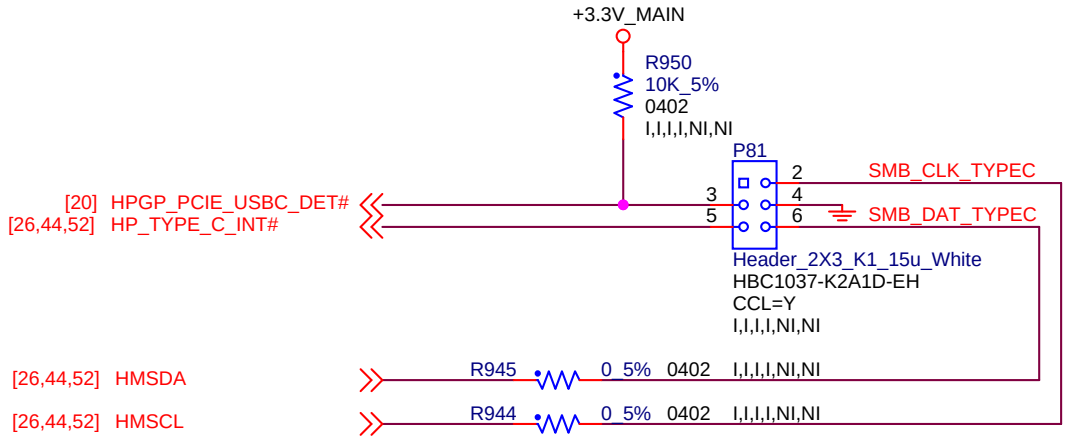
Title: LEGACY-IO

Size	Document Number	Rev
A	901015-000	A

Date: Wednesday, November 09, 2016 | Sheet 31 of 92

ENT15 USBC Header

Note 1



Design Note

Note 1

Only Applied to D800 and D600

Footprint Only for D400

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	X
Crux	X

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Title: LEGACY-IO

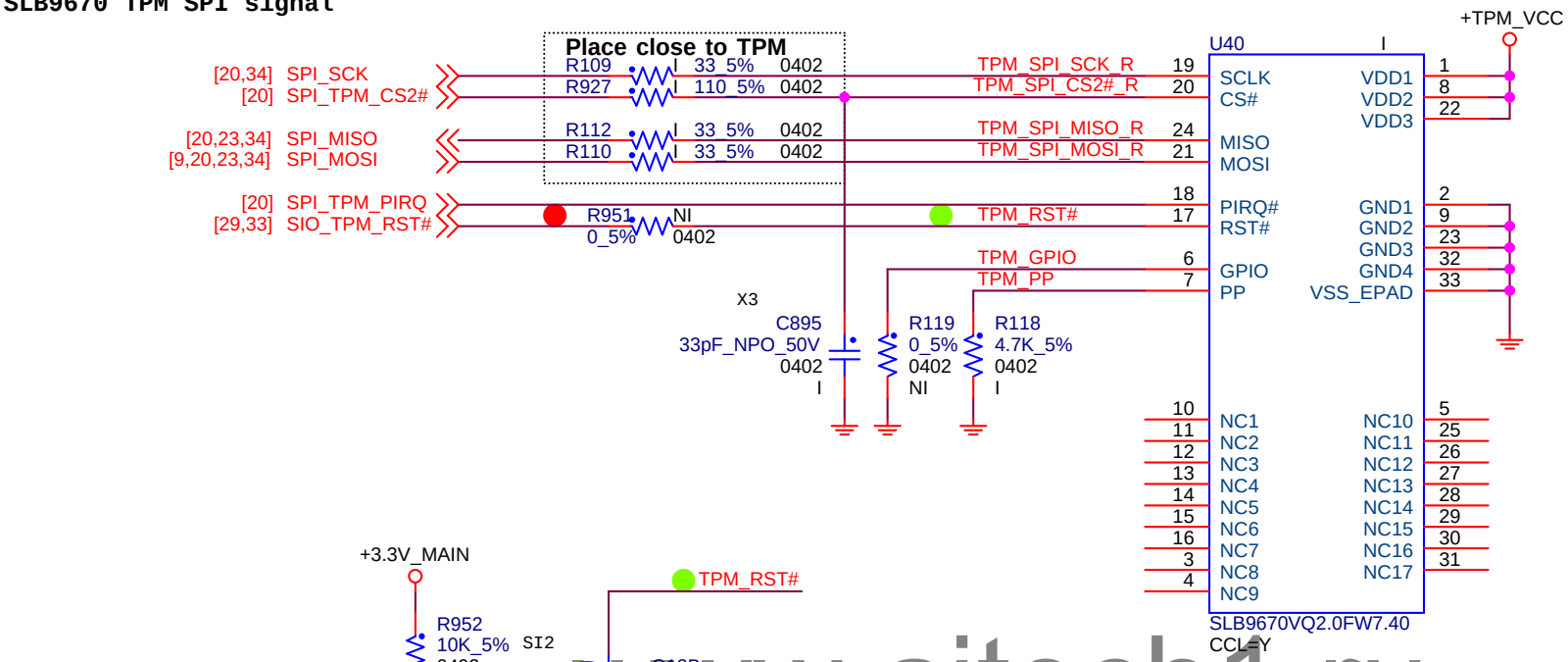
Size	Document Number	Rev
A	901015-000	A

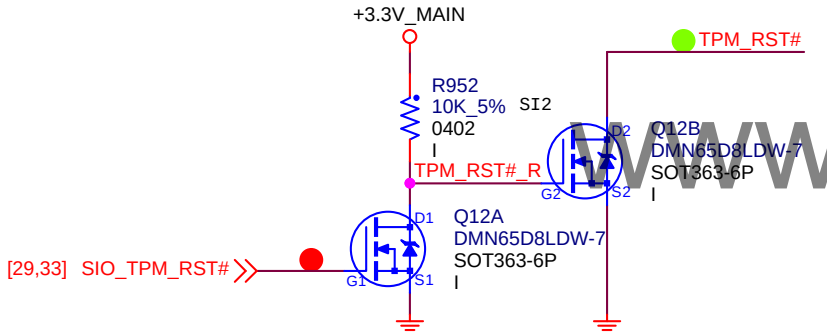
Date: Wednesday, November 09, 2016 Sheet 32 of 92

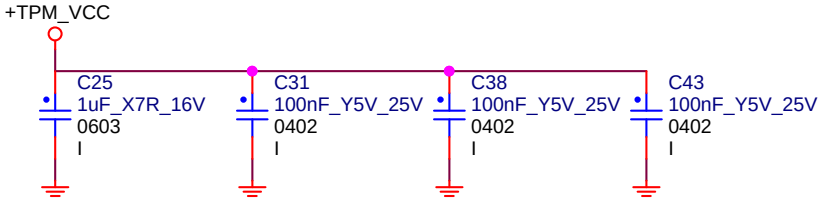
TPM

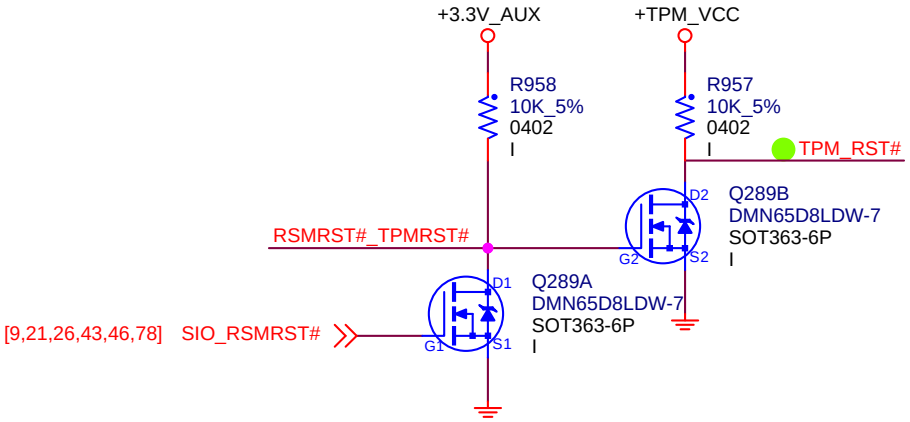
For SLB9670 TPM SPI signal

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V









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Title	TPM	
Size A	Document Number 901015-000	Rev A
Date: Wednesday, November 09, 2016	Sheet 33 of 92	

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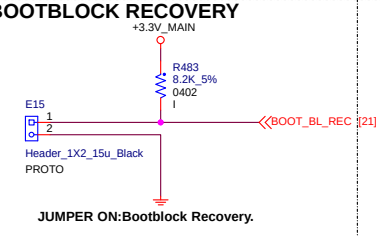
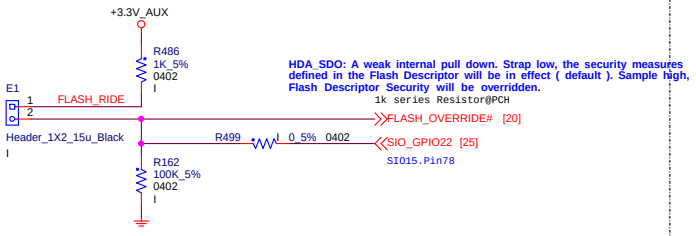
BIOS

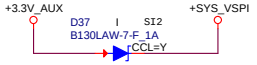
BOOTBLOCK RECOVERY



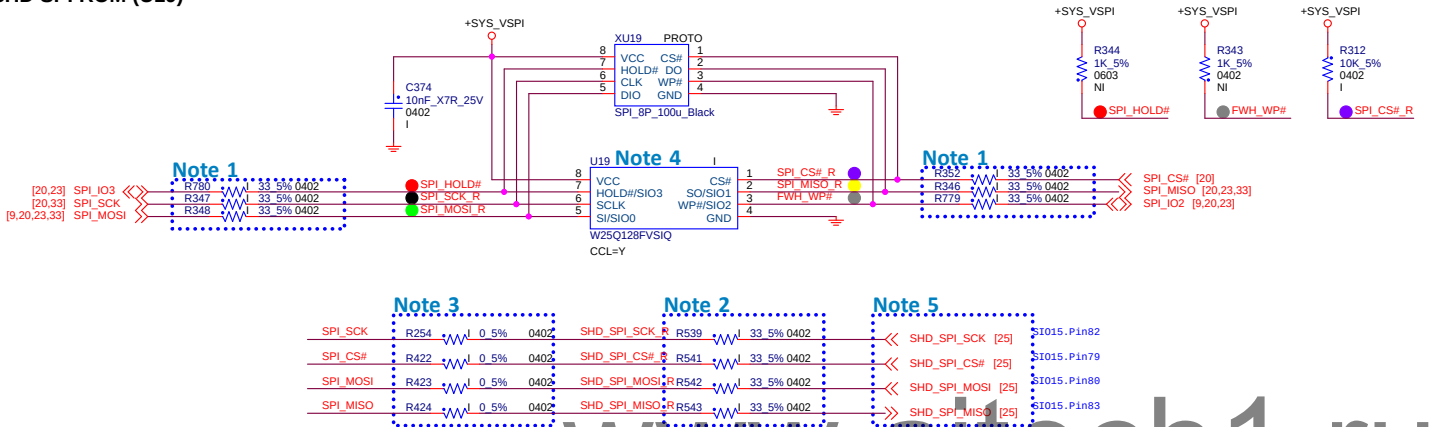
Flash Descriptor Table Override (E1)



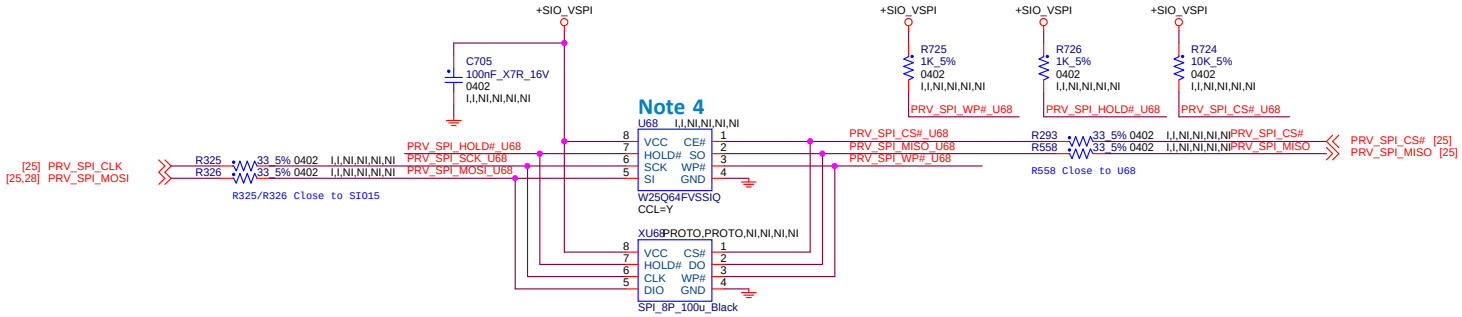
SPI ROM POWER



PCH+ SIO SHD SPI ROM (U19)



SIO15 Privately SPI ROM (U68)



Design Note

Note 1

Place R780 close to U19 within 1000 mils
Place R347 close to U19 within 1000 mils
Place R348 close to U19 within 1000 mils
Place R352 close to U19 within 1000 mils
Place R346 close to U19 within 1000 mils
Place R779 close to U19 within 1000 mils

Note 2

Place R539 close to SIO15.Pin82 within 1000 mils
Place R541 close to SIO15.Pin79 within 1000 mils
Place R542 close to SIO15.Pin80 within 1000 mils
Place R543 close to SIO15.Pin83 within 1000 mils

Note 3

Place R254 at Tpoint
Place R422 at Tpoint
Place R423 at Tpoint
Place R424 at Tpoint

Note 4

U19 and U68 Property
NPI: DIP
MVB: SMD

Note 5

SIO SHD SPI routing is treat as 2nd flash device

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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Title: BIOS

Size: Custom | Document Number: 901015-000 | Rev: A

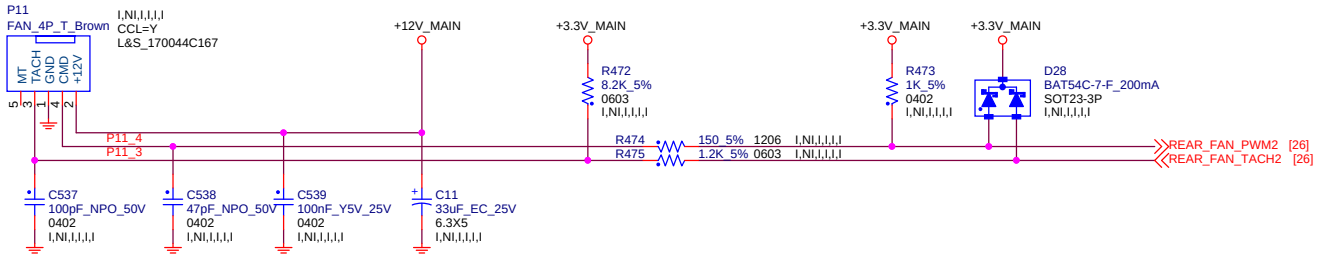
Date: Wednesday, November 09, 2016 | Sheet 34 of 92

Rear Chasis FAN

Color: Red

D8 SFF would not support system FAN

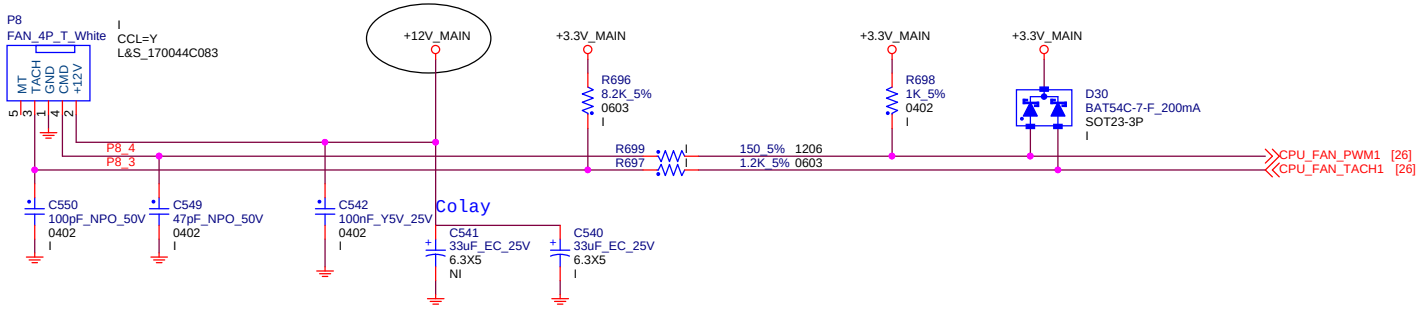
Foxconn header footprint has been updated. Need to check. [P8/P11/P125]



CPU FAN

Color: White

Foxconn header footprint has been updated. Need to check. [P8/P11/P125]



Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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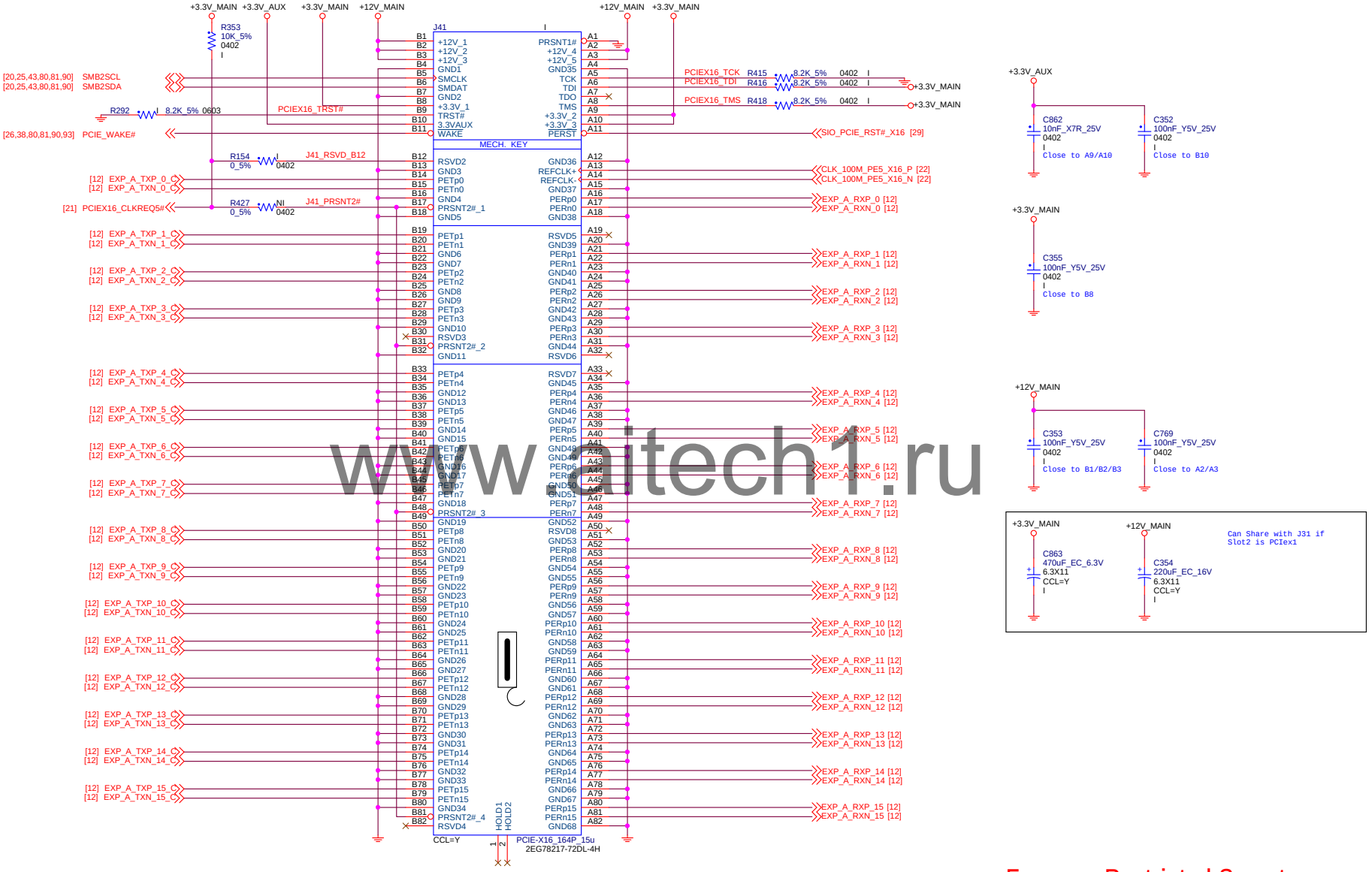
Title: FAN HEADERS

Size: Custom | Document Number: 901015-000 | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 35 of 92

PCI EXPRESS X16 SLOT1



SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements

SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs

SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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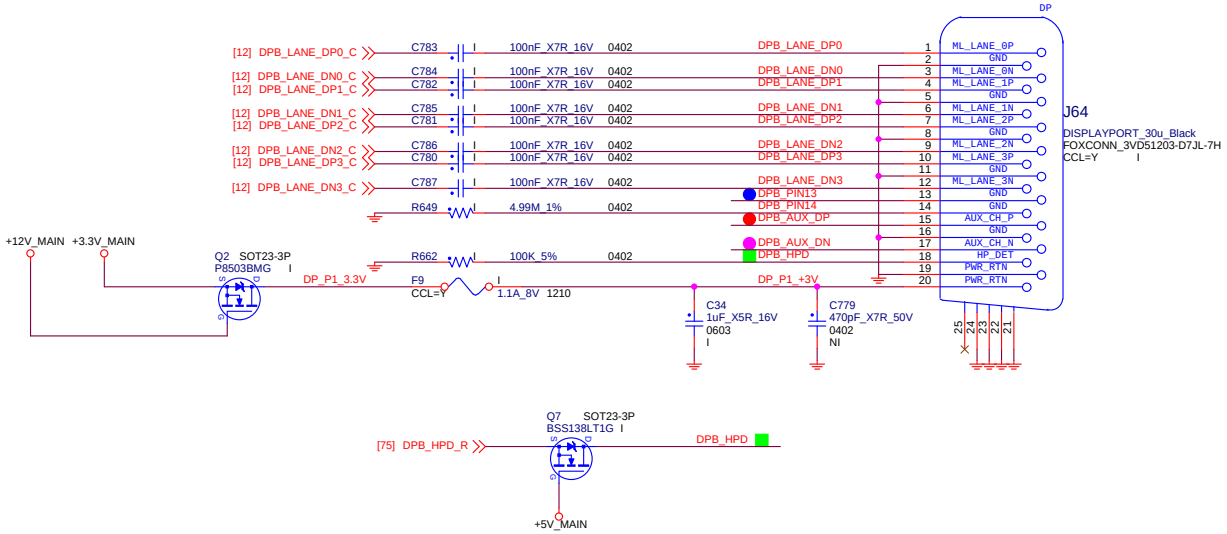
Title PCIE - x16

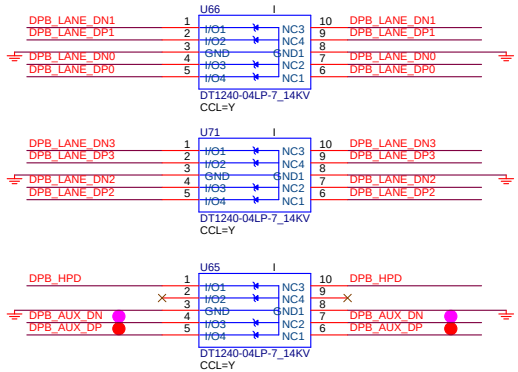
Size Custom | Document Number 901015-000 | Rev A

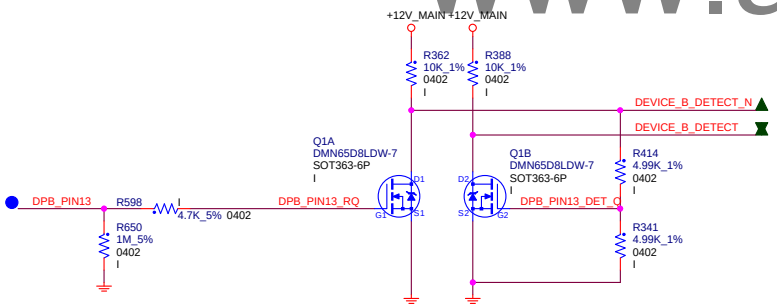
Date: Wednesday, November 09, 2016 | Sheet 36 of 92

DISPLAY PORT

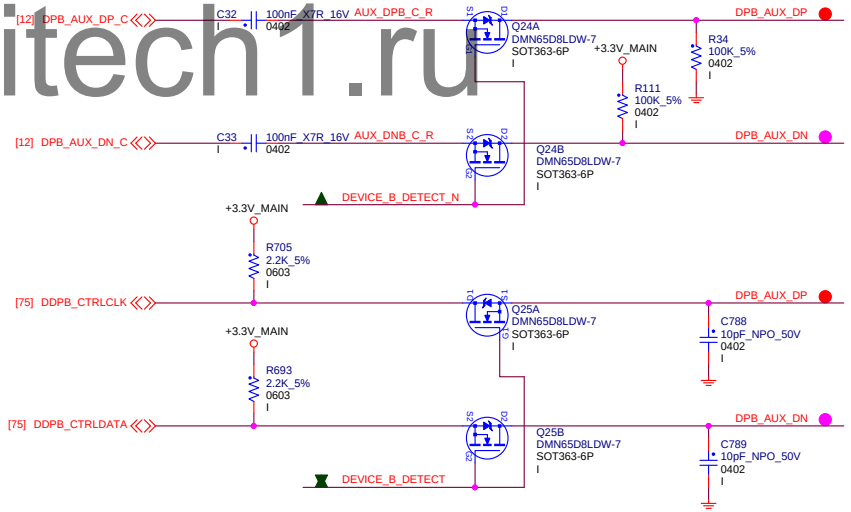


ESD suppressor





PIN13		FUNCTION
DP	DONGLE	
L	X	DEVICE_C_DETECT
X	H	DEVICE_C_DETECT_N



Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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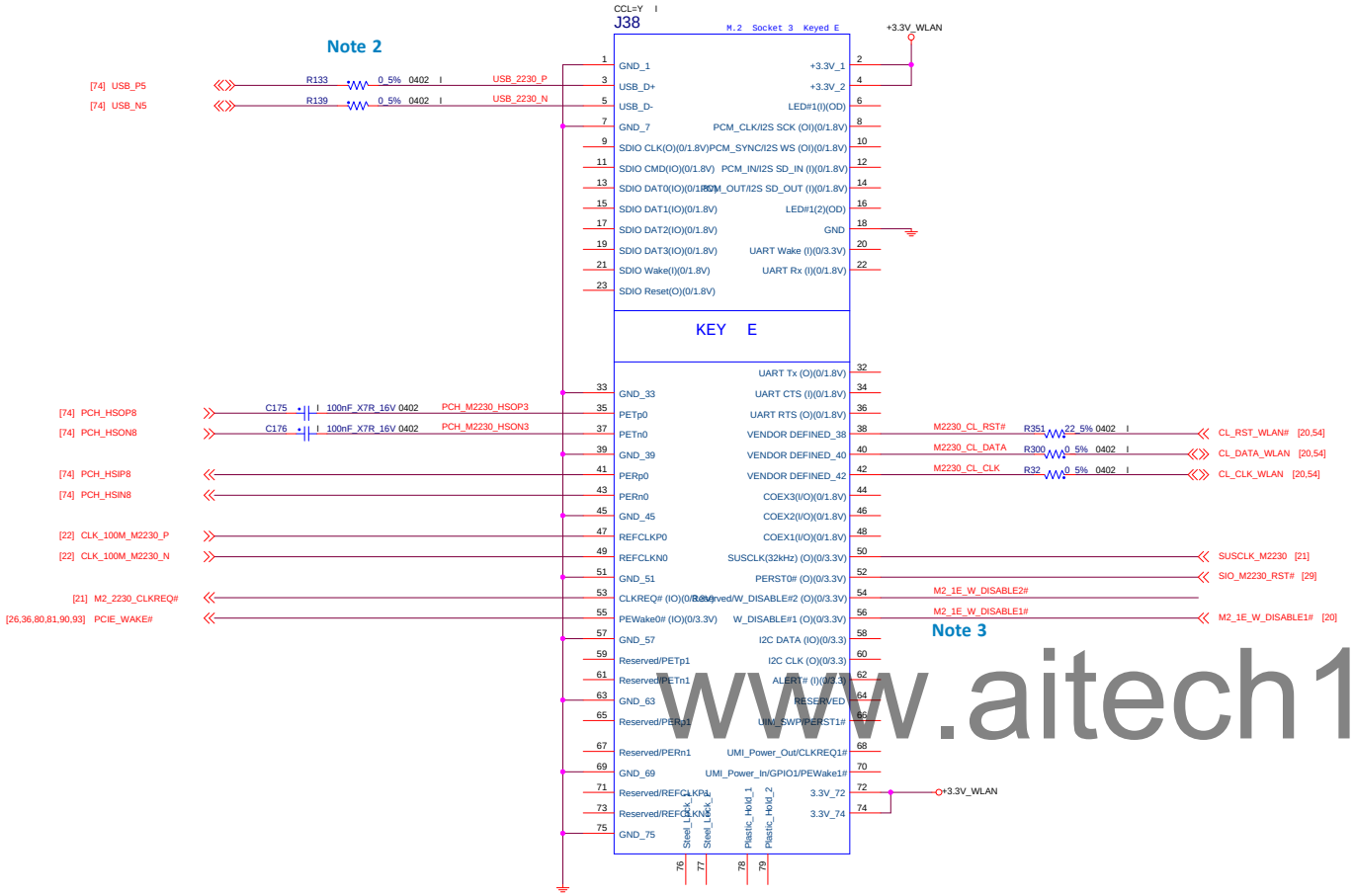
Title: DISPLAY PORT 1

Size: Custom | Document Number: 901015-000 | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 37 of 92

M2_2230_SOCKET1-KEYE



Design Note

Note 1

Place C26 close to J38.2 and J38.4
Place C750 close to J38.2 and J38.4
Place C16 close to J38.2 and J38.4
Place C78 close to J38.72 and J38.74
Place C749 close to J38.72 and J38.74
Place C15 close to J38.72 and J38.74
Place C751, C855, C756 close to J38

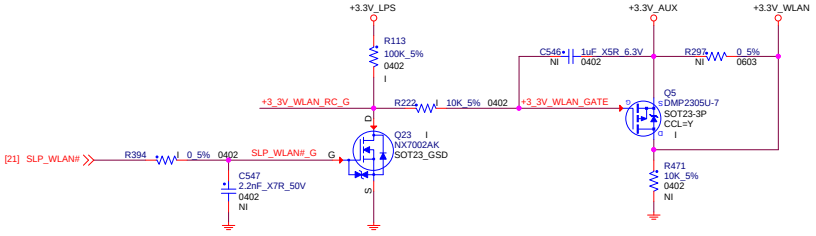
Note 2

Place L7, R133, R139 close to J38

Note 3

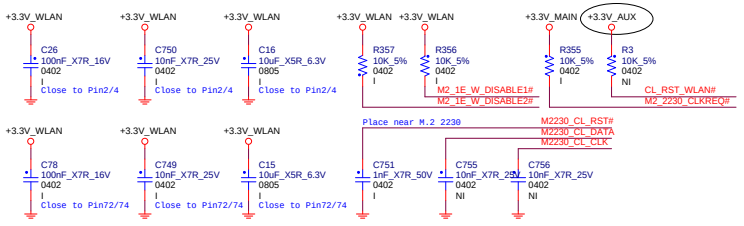
Pin56 OF J38 allows Hardware to disable WI-FI
Pin54 OF J38 allows Hardware to disable BT

M.2 2230 Power Circuit



M.2 HW Config and Power Cap

Note 1



Foxconn Restricted Secret

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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Title: M2_2230_SOCKET1-KEYE

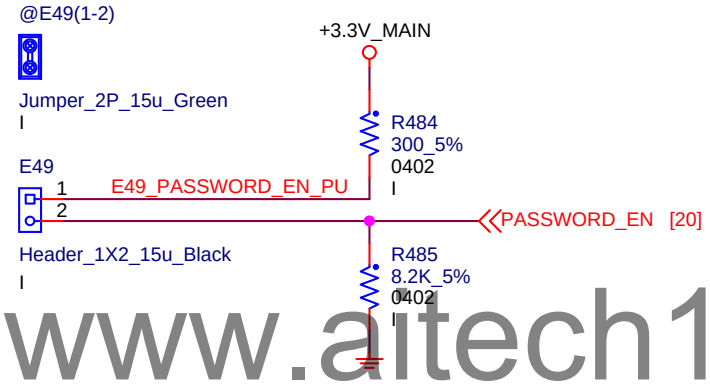
Size	Document Number	Rev
C	901015-000	A

Date: Wednesday, November 09, 2016 Sheet 38 of 92

PASSWORD JUMPER

Have to tacke care the location

JUMPER ON:PASSWORD ENABLE



Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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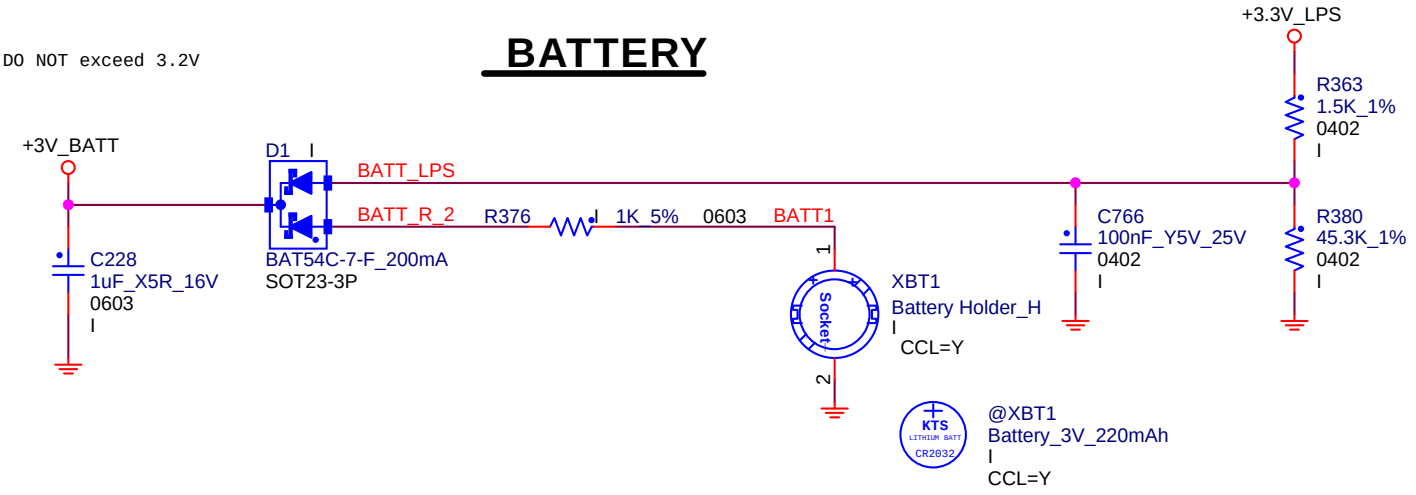
Title: **Security**

Size	Document Number	Rev
A	901015-000	A

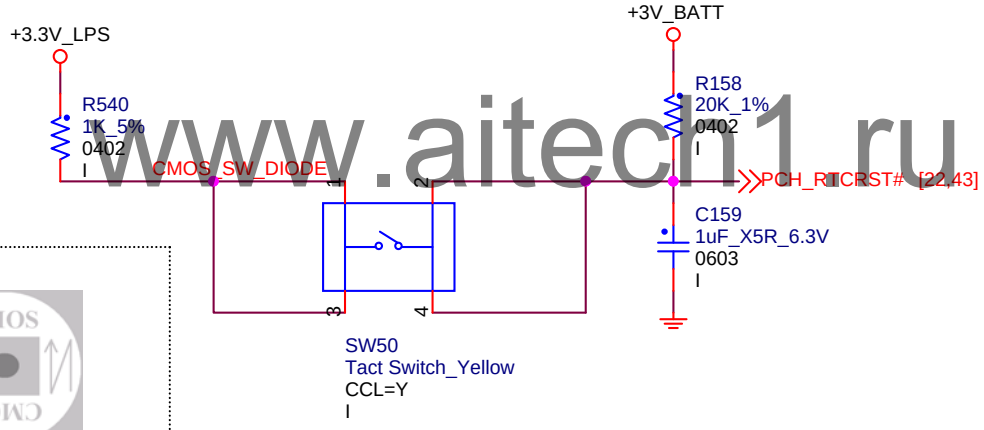
Date: Wednesday, November 09, 2016 | Sheet 39 of 92

BATTERY

DO NOT exceed 3.2V



CLEAR CMOS BUTTON



CAD NOTE:
The PCB must have this silkscreen for HPQ

This circuit disables the clear CMOS function when system is powered

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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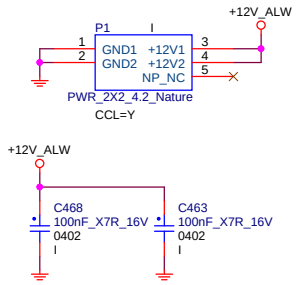
Title: **Battery/CMOS**

Size	Document Number	Rev
A	901015-000	A

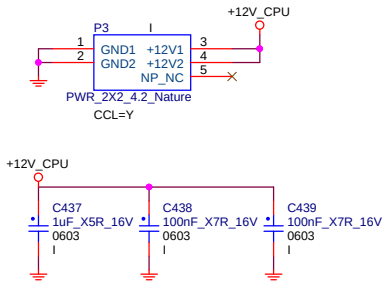
Date: Wednesday, November 09, 2016 | Sheet 40 of 92

PWR CON/AUXLED

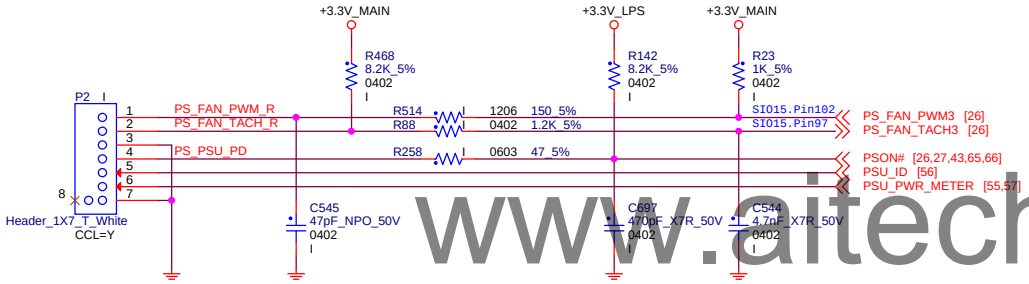
System Power Connector (P1)



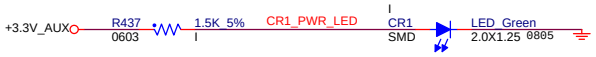
CPU Power Connector (P3)



HP 12V Power Connector (P2)

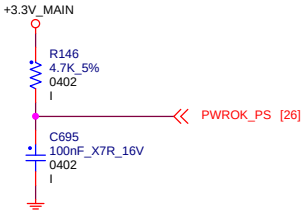


Aux Power LED - Ent11



PWROK

Note 1



Design Note

Note 1:
Place R146 close to SIO Side to minimize the trace length

Foxconn Restricted Secret

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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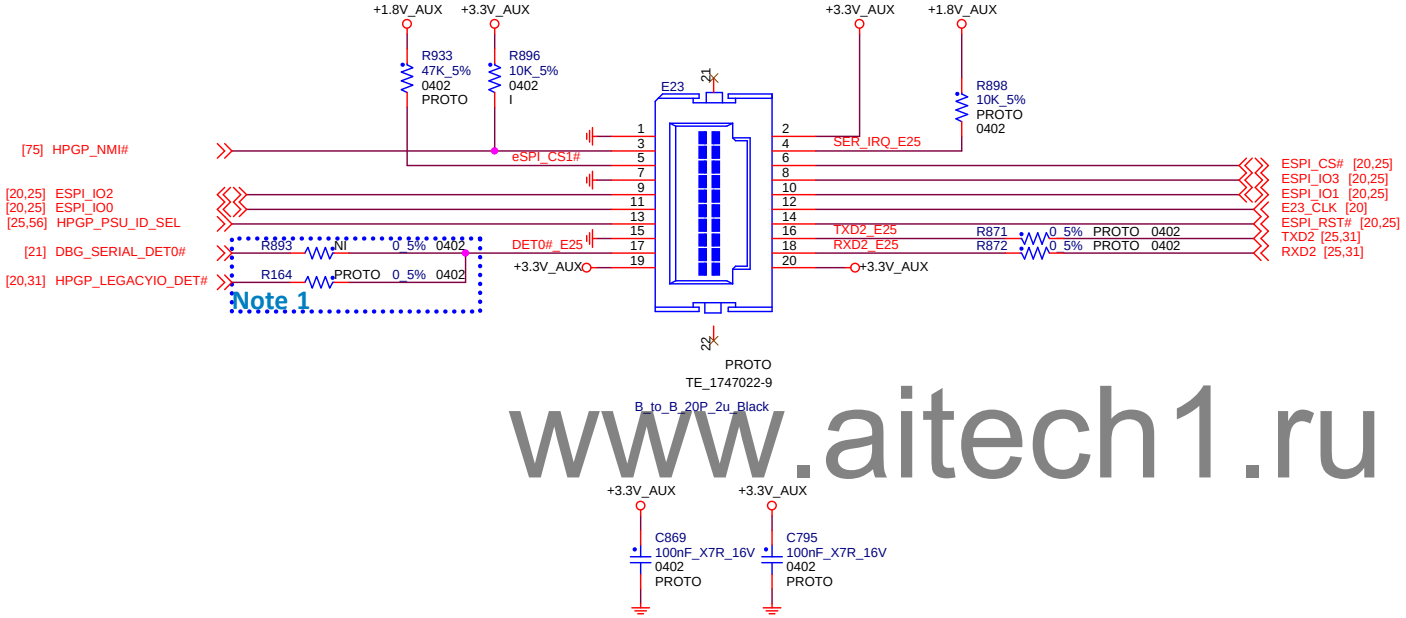
Title: PWR CON/AUXLED

Size: Custom | Document Number: 901015-000 | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 41 of 92

PLATFORM DEBUG HEADER



Design Note

Note 1

If COM2 is used for option module, both option and debug header connect with same GPIO detection signal

Note 2

For LPC
E23.Pin2 connect to SER_IRQ, and NI R898
E23.Pin5, Change to PD with 47Kohm

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

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Title: PLATFORM DEBUG

Size	Document Number	Rev
B	901015-000	A

Date: Wednesday, November 09, 2016 Sheet 42 of 92

PCA LEDs

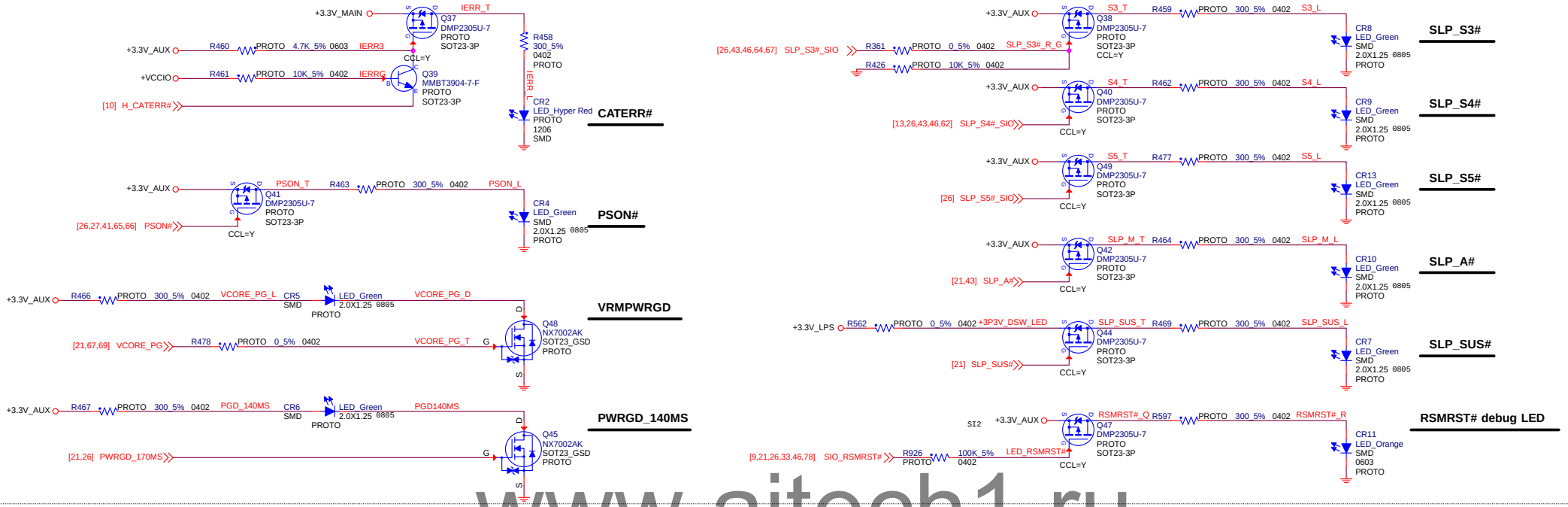
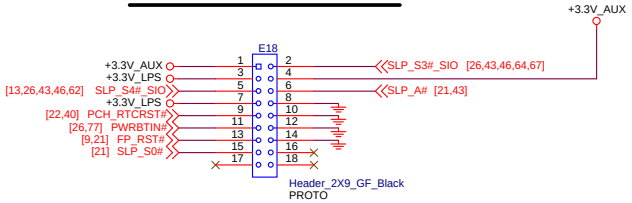


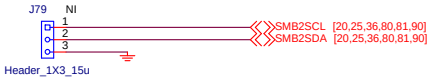
Table 27-4. Pin Location for Dual-in-Line header

Signal Name	Pin			Pin	Signal Name
VccSus3_3	1	o	o	2	SLP_S3#
VccDSW3_3	3	o	o	4	SLP_S5#
SLP_S4#	5	o	o	6	SLP_A#
VccDSW3_3	7	o	o	8	GND
RTCRST#	9	o	o	10	GND (for RTCRST#)
PWRBTN#	11	o	o	12	GND (for PWRBTN#)
SYS_RESET#	13	o	o	14	GND (for SYS_RESET#)
SLP_S0#	15	o	o	16	NC
NC	17	o		18	NC

METS/APS TEST HEADER



ME DEBUG HEADER



Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	V
Crux	V

Foxconn Restricted Secret

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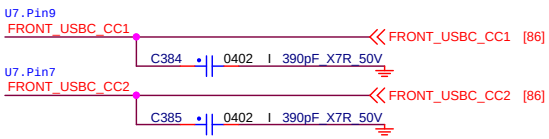
Title: LEDs/METS

Size: Custom | Document Number: 901015-000 | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 43 of 92

FRONT TYPEC PD Controller - DFP Only

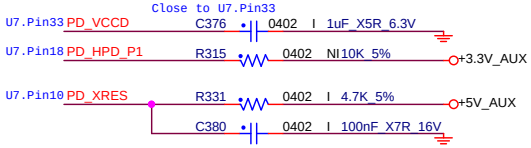
Leakage Voltage Protection for CC



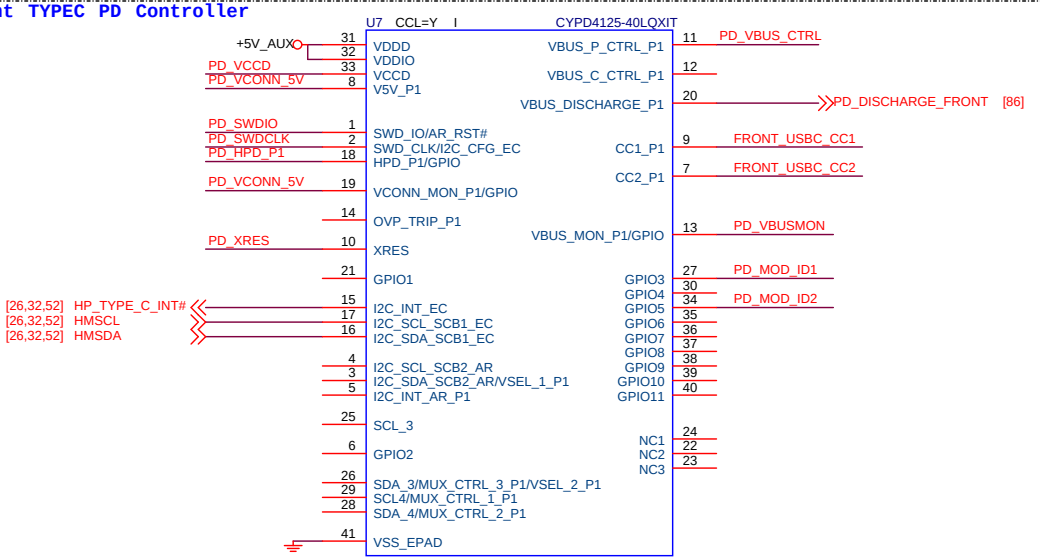
SMBus/INT# Pull-Up

Already PU @ SIO Page26

PD Controller HW Setting



Front TYPEC PD Controller



Design Note

Note 1

DFP Mode:
ID1 = L5 ; ID2 = L1
DFP+DP Mode
ID1 = L5 ; ID2 = L2

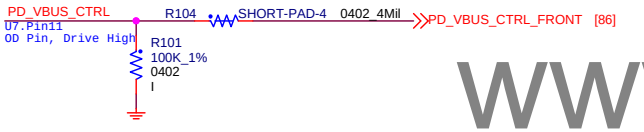
L0 = 0V
L1 = VDD/8
L2 = 2VDD/8
L3 = 3VDD/8
L4 = 4VDD/8
L5 = 5VDD/8
L6 = 6VDD/8
L7 = 7VDD/8

Note 2

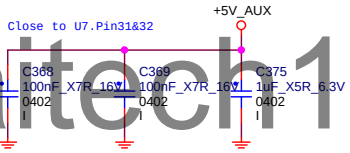
SMBUS ADDRESS
08 (when SWD CLK = floating)
40 (when SWD CLK = low)
42 (when SWD CLK = high)

The first will be 40 and the second will be 42
If have 2 Type-C controllers:
- 40 will be Dual Port controller.
- 42 will be Single Port controller.

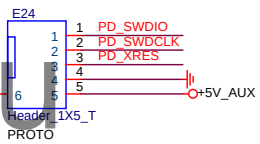
PD Controller HW Setting
Change List 1&2



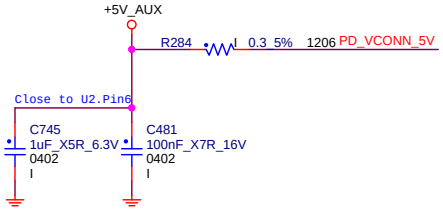
PD VIN Decoupling CAP



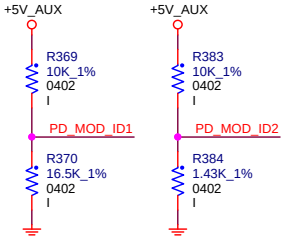
Debug Header



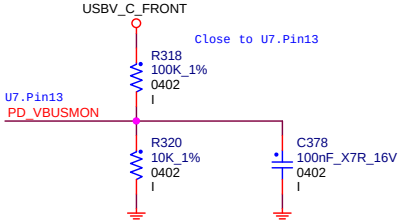
OCP Protection for VCONN



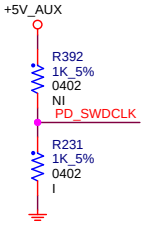
MOD_ID Selection
Note 1
Change List 3



VBUS Monitor



SMBus Address Config.
Note 2



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Change List

Following CCG4 Unified Schematics_HPv7_040816 to update
1. Remove OVP Trip From CCG4 cirucit. OVP can be floating
2. VBUS CTRL directly connect to Power Switch.
3. Add MOD_ID select info for difference configuration mode Please refer to Design Note
4. Remove R104, U6, C58 for Item1&2 5. Add R369, R383, R370, R384 for Item3

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	X
Crux	X

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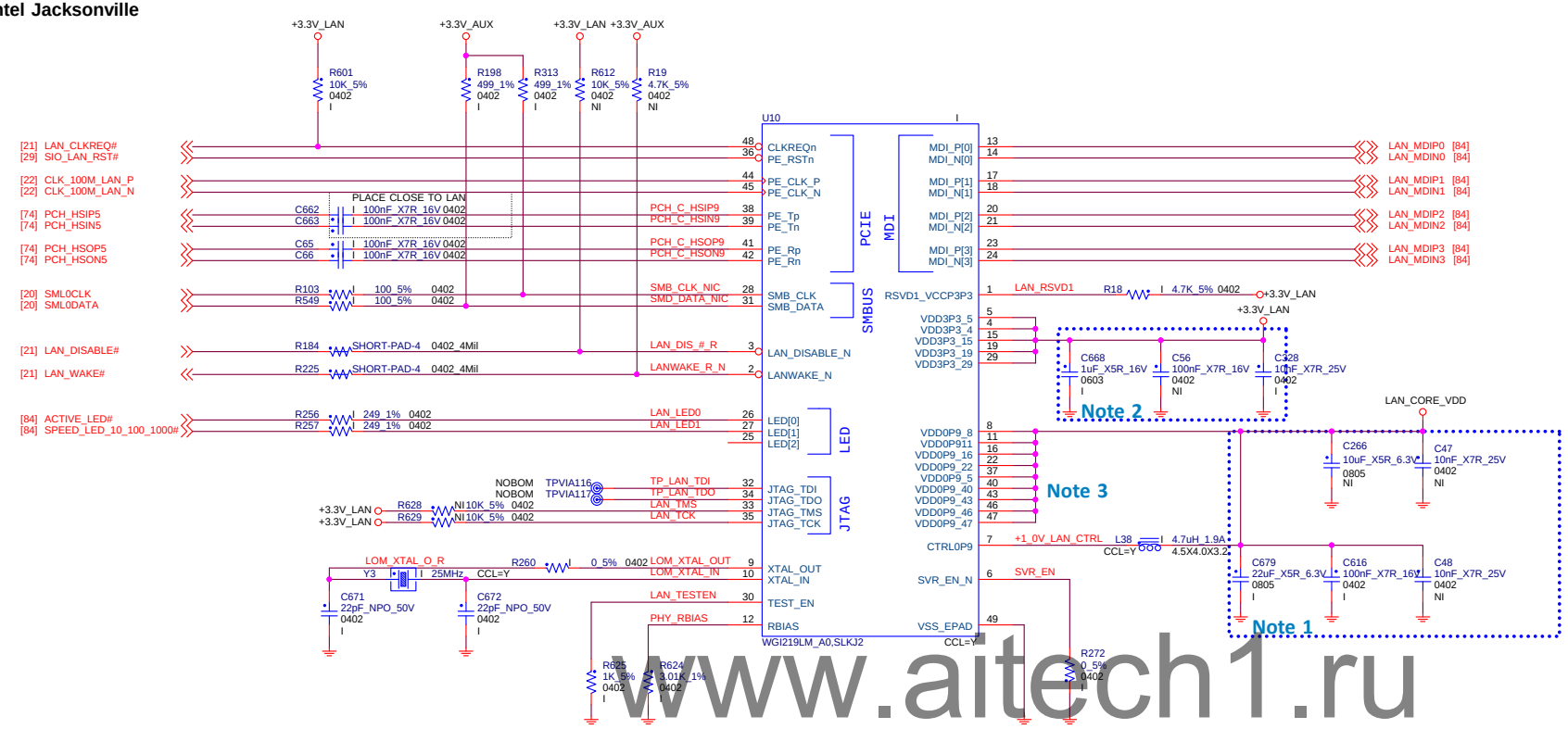
Title: D8D6_CCG4 Controller

Size B | Document Number 901015-000 | Rev A

Date: Wednesday, November 09, 2016 | Sheet 44 of 92

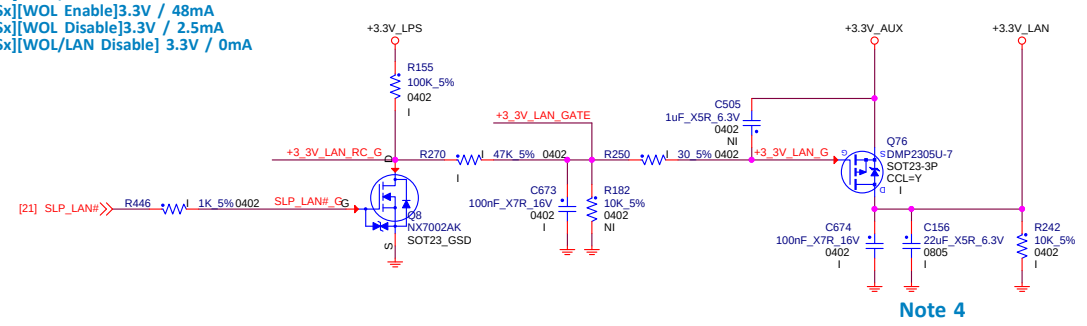
D8D6_Intel Jacksonville

Intel Jacksonville

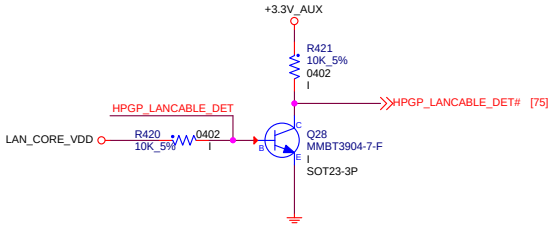


LAN Power Circuit

Power Consumpt i on
[S0] 3.3V / 132 mA
[Sx][WOL Enable]3.3V / 48mA
[Sx][WOL Disable]3.3V / 2.5mA
[Sx][WOL/LAN Disable] 3.3V / 0mA



LAN Cable Detect Circuit



Design Note

Note 1
C266, C679, C616, C48 Place close to U10
C47 Place close to U10.16
C48 Place close to U10.22

Note 2
C328 Place close to U10.15
C56, C668 Place close to U10

Note 3
Trace keep short and wide

Note 4
C156 PLACE NEAR VDD PINS
R242 PLACE NEAR Pin5.

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	X
Crux	X

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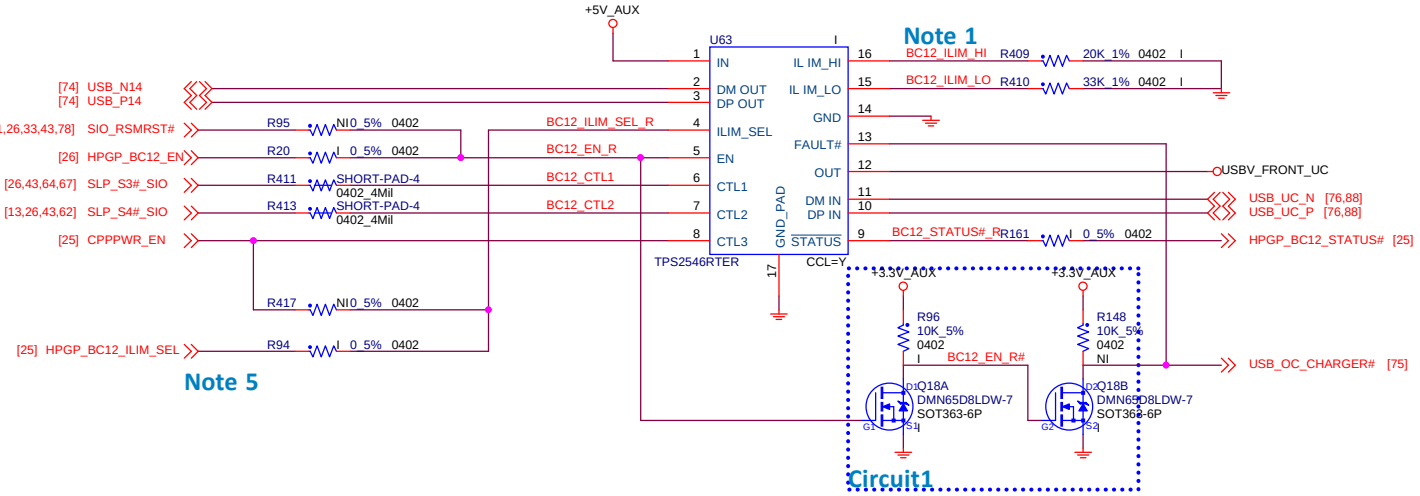
Title: D8D6_Intel Jacksonville

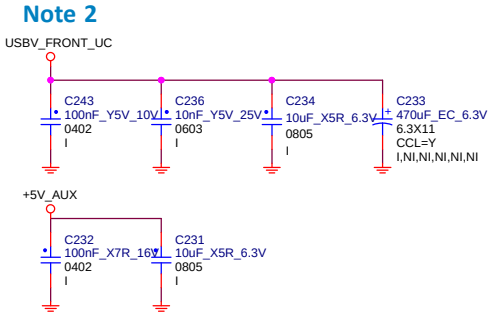
Size: Custom | Document Number: 901015-000 | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 45 of 92

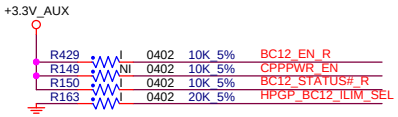
USB CHARGER



INPUT/OUTPUT CAP



USB Charger HW Config



Design Note

Note 1
Current limit for ILIM_HI (CDP/DCP mode)=2510mA
Current limit for ILIM_LO (SDP mode)=1525mA
TI2546
Ishort = 50500/RILM

Note 2
Place C232 and C231 close to U63

Place C243, C236, C235, C234, and C233 close to U63

Note 3
USB Charging mode selection in System Status

State \ bit	CTL1 SLP_S3#	CTL2 SLP_S4#	CTL3	ILIM_SEL	Mode	ILIM
S0	1	1	1	1	CDP	2510mA
S0	1	1	0	0	SDP	1525mA
S3	0	1	1	1	DCP_AUTO	2510mA
S3	0	1	0	0	SDP	1525mA
S4/S5	0	0	1	1	DCP	2510mA
S4/S5	0	0	0	0	TURN OFF	1525mA

Note 4
BOM Option: To enable/disable Charger Kill and Throttling

State \ bit	PIN4 PIN8	PIN5 PIN13	PIN9
Disable	I: R417 NI: R94	I: R95 NI: R20/Circuit1	NI: R161, R150
Enable	SIO_VSPI: 3.3V I: R94 NI: R417	I: R20/Circuit1 NI: R95	I: R161, R150

Note 5
If SIO_VSPI is 1.8v level, it need one level shif for PIN4

Note 6
NI R148 due to duplicate PU on R448.

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	X
Crux	X

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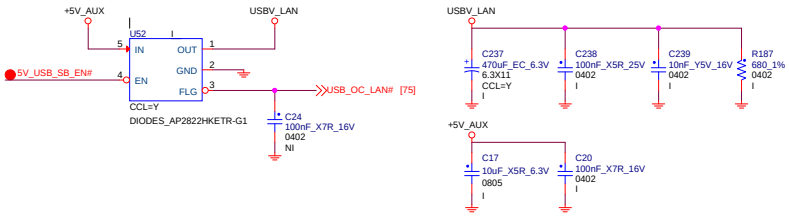
Title: D8D6_USB CHARGER

Size: Custom | Document Number: 901015-000 | Rev: A

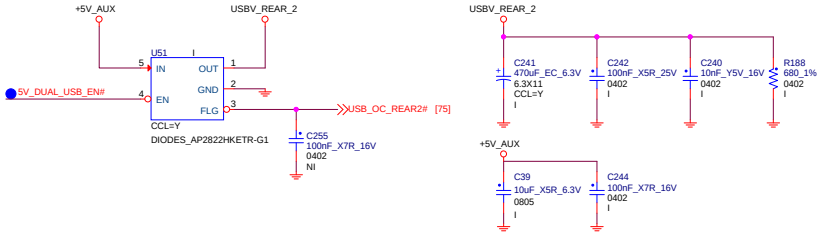
Date: Wednesday, November 09, 2016 | Sheet 46 of 92

USB POWER

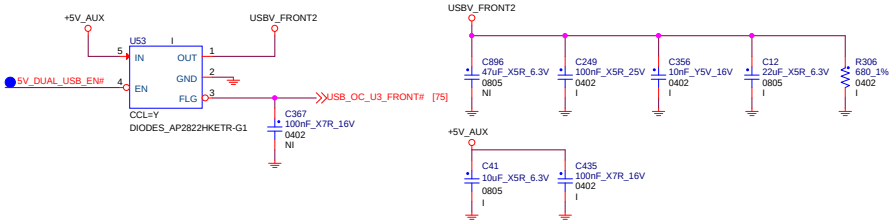
LAN+USB2x2



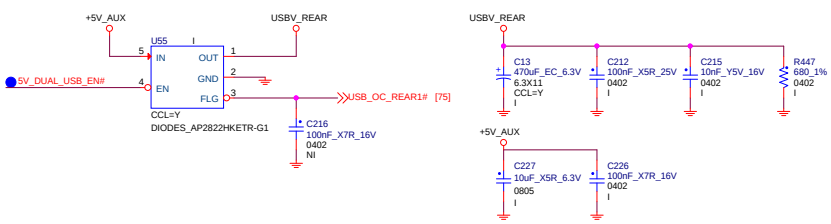
REAR USB POWER FOR USB3.0x2



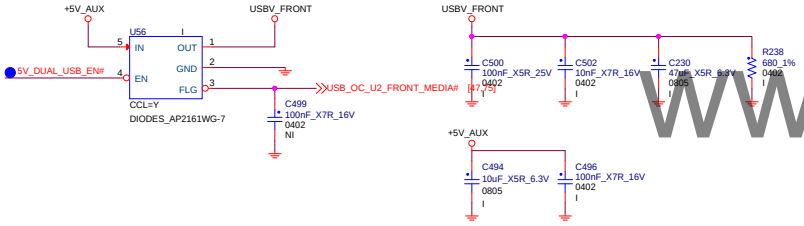
FRONT(P26) USB POWER for USB3.0



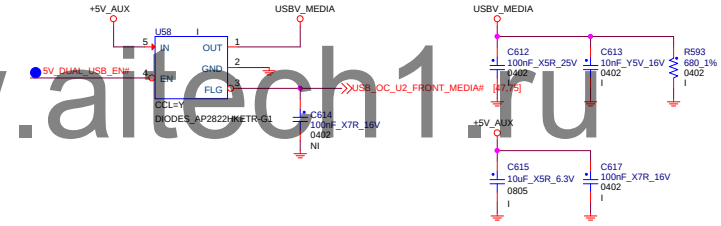
REAR USB POWER FOR USB3.0x2

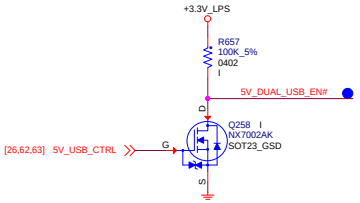


FRONT(P24) USB POWER for USB2.0



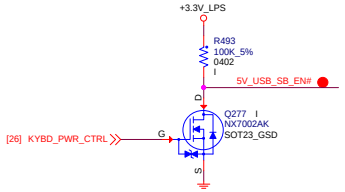
MEDIA(P152) USB POWER For USB3





GPIO Power Well = DSW
or SUS
Need to use SIO GPIO

GPIO	5V_USB_SB_EN#
H	Swtich On
L	Swtich Off



Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	X
Crux	X

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Title: D8D6_USB POWER

Size: C | Document Number: 901015-000 | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 47 of 92

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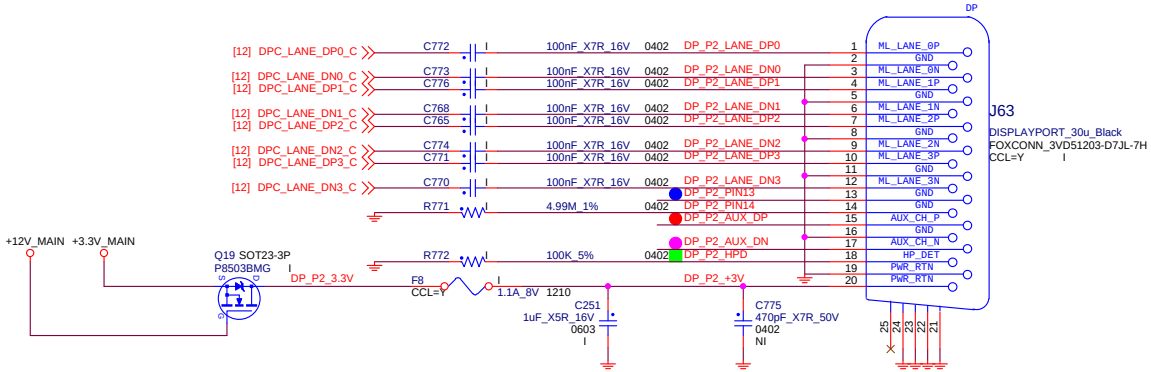
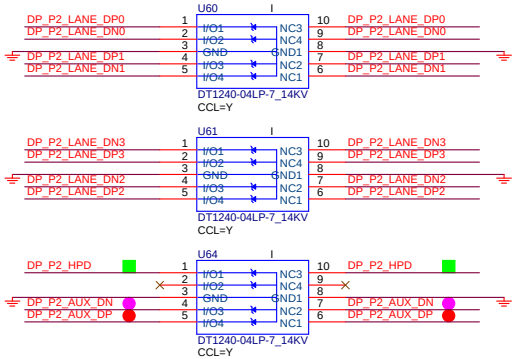
Size	Document Number	Rev
B	901015-000	A

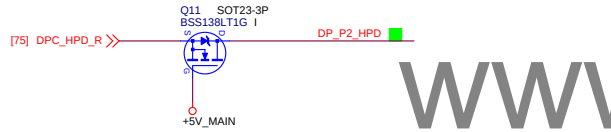
Date: Wednesday, November 09, 2016 Sheet 48 of 92

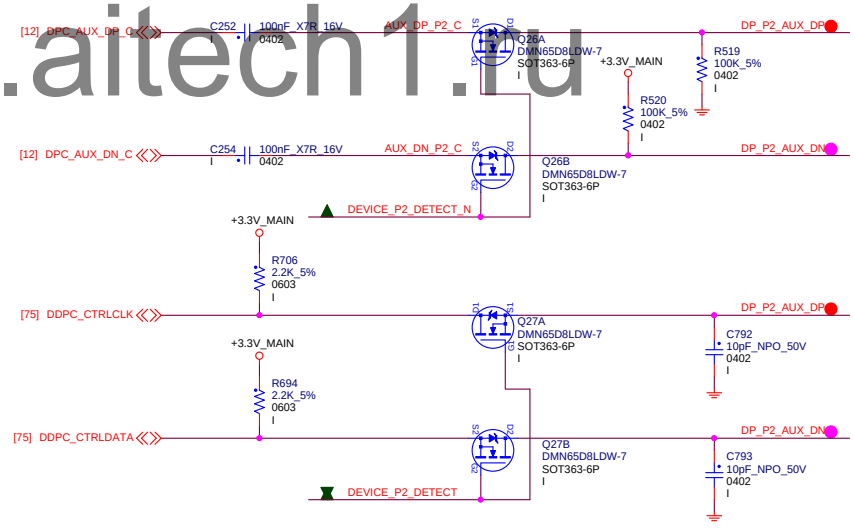
DISPLAY PORT

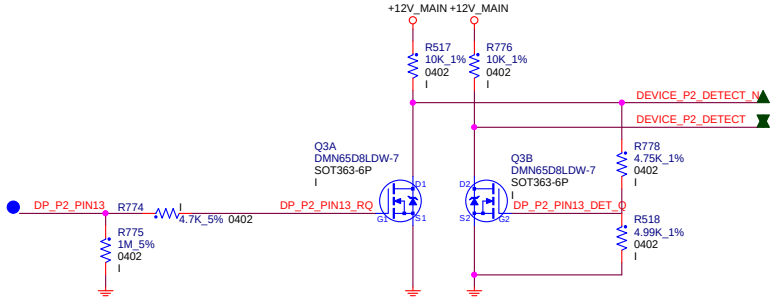


ESD suppressor









PIN13		FUNCTION
DP	DONGLE	
L	X	DEVICE_D_DETECT
X	H	DEVICE_D_DETECT_N

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	X
Crux	X

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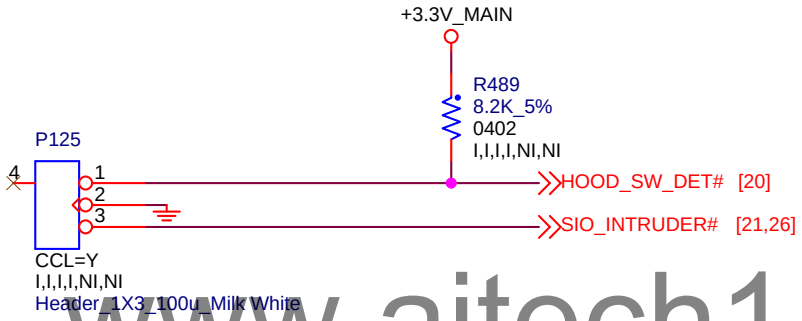
Title D8D6_DISPLAY PORT 2

Size Custom | Document Number 901015-000 | Rev A

Date: Wednesday, November 09, 2016 | Sheet 49 of 92

HOOD SENSE CIRCUT

Have to tacke care the location



Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	X
Crux	X

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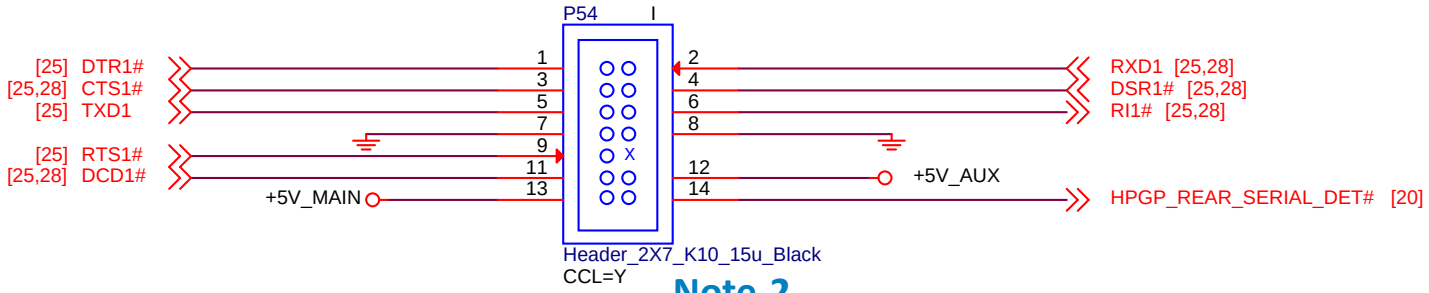
Title: **D8D6_HHOD SENSE**

Size	Document Number	Rev
A	901015-000	A

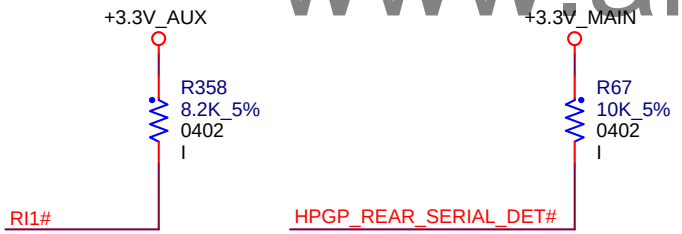
Date: Wednesday, November 09, 2016 | Sheet 50 of 92

SINGLE COM PORT Note 1

COMA



HW PU/PD Config



Design Note

Note 1
Only Applied to D800 and D600

Note 2
Using PortA = Black Header
Using PortB = White Header

Note 3

PINOUT

P52
1ST Serial

1 DTR#	2 RXD
3 CTS#	4 DSR#
5 TXD	6 RI#
7 GND	8 GND
9 RST#	10 KEY
11 DCD#	12 +5V_VSB
13 +5V_MAIN	14 COMM x DET#

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	X
Crux	X

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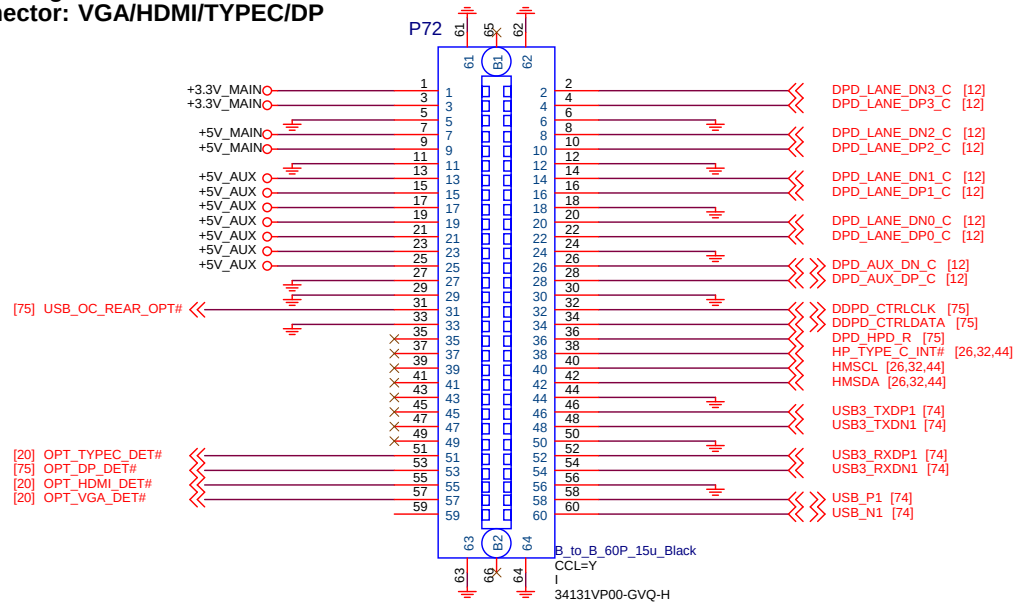
Title: D8D6_Single COM Port

Size	Document Number	Rev
A	901015-000	A

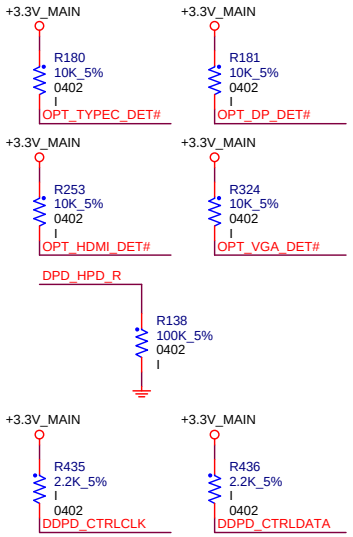
Date: Wednesday, November 09, 2016 | Sheet 51 of 92

Rear Opt i on Car d Note 1

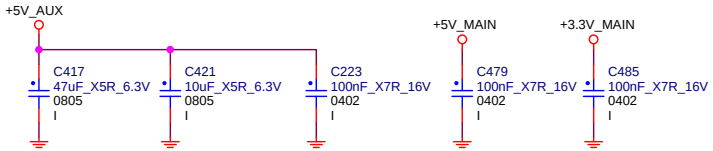
Rear Daughter Card
Connector: VGA/HDMI/TYPEC/DP



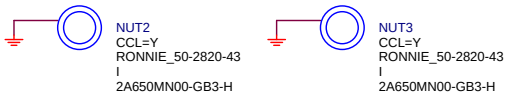
Rear Daughter Card
HW PU/PD Config



Rear Daughter Card
Decoupling CAP



Rear Daughter Card
Stand Off



Design Note

Note 1
Only Applied to D800 and D600

TABLE 58
P72/P73 - EXTEN I/O PIN DEFINAION - ENT17

Pin #	Signal Name	Signal Name	Pin #
1	+3.3V	DDI_TXP0	2
3	+3.3V	DDI_TXN0	4
5	GND	GND	6
7	+5V	DDI_TXP1	8
9	+5V	DDI_TXN1	10
11	GND	GND	12
13	+5V_AUX	DDI_TXP2	14
15	+5V_AUX	DDI_TXN2	16
17	+5V_AUX	GND	18
19	+5V_AUX	DDI_TXP3	20
21	+5V_AUX	DDI_TXN3	22
23	+5V_AUX	GND	24
25	+5V_AUX	DDI_AUXP	26
27	GND	DDI_AUXN	28
29	GND	GND	30
31	GND	CTRCLK	32
33	GND	CTLDATA	34
35	CTS#	DP_HPD #	36
37	DTR#	USB Type-C INT#	38
39	DSR#	SMBus_CLK(AUX mode)	40
41	DCD#	SMBus_DATA(AUX mode)	42
43	TXD	GND	44
45	RXD	USB 3.1 TX+	46
47	RTS#	USB 3.1 TX-	48
49	RI#	GND	50
51	USB Type-C card detention#	USB 3.1 RX+	52
53	DP Card detention#	USB 3.1 RX-	54
55	HDMI card detection#	GND	56
57	VGA card detection#	USB 2.0 D+	58
59	Serial port detention#	USB 2.0 D-	60

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	X
Crux	X

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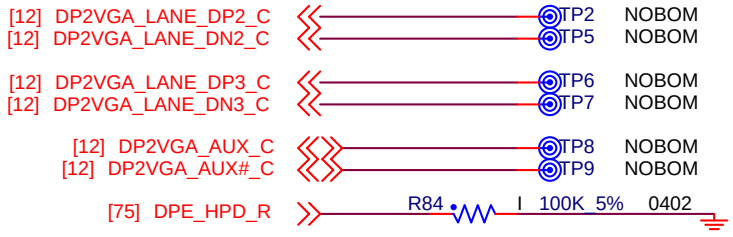
Title: D8D6_Rear Option Card

Size	Document Number	Rev
B	901015-000	A

Date: Wednesday, November 09, 2016 Sheet 52 of 92



Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	X
Crux	X

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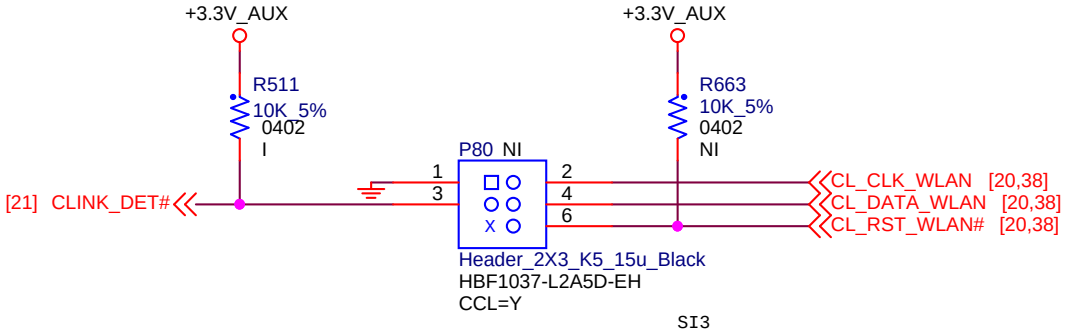
Title
D8D6_NC NET TEST POINT

Size	Document Number	Rev
A	901015-000	A

Date: Wednesday, November 09, 2016 Sheet 53 of 92

CLINK Header

Note 1



Design Note

Note 1

D8 Footprint Only

D6 Footprint Only

Project	
Andromeda	V
Apus	V
Auriga	V
Aries	V
Carina	X
Crux	X

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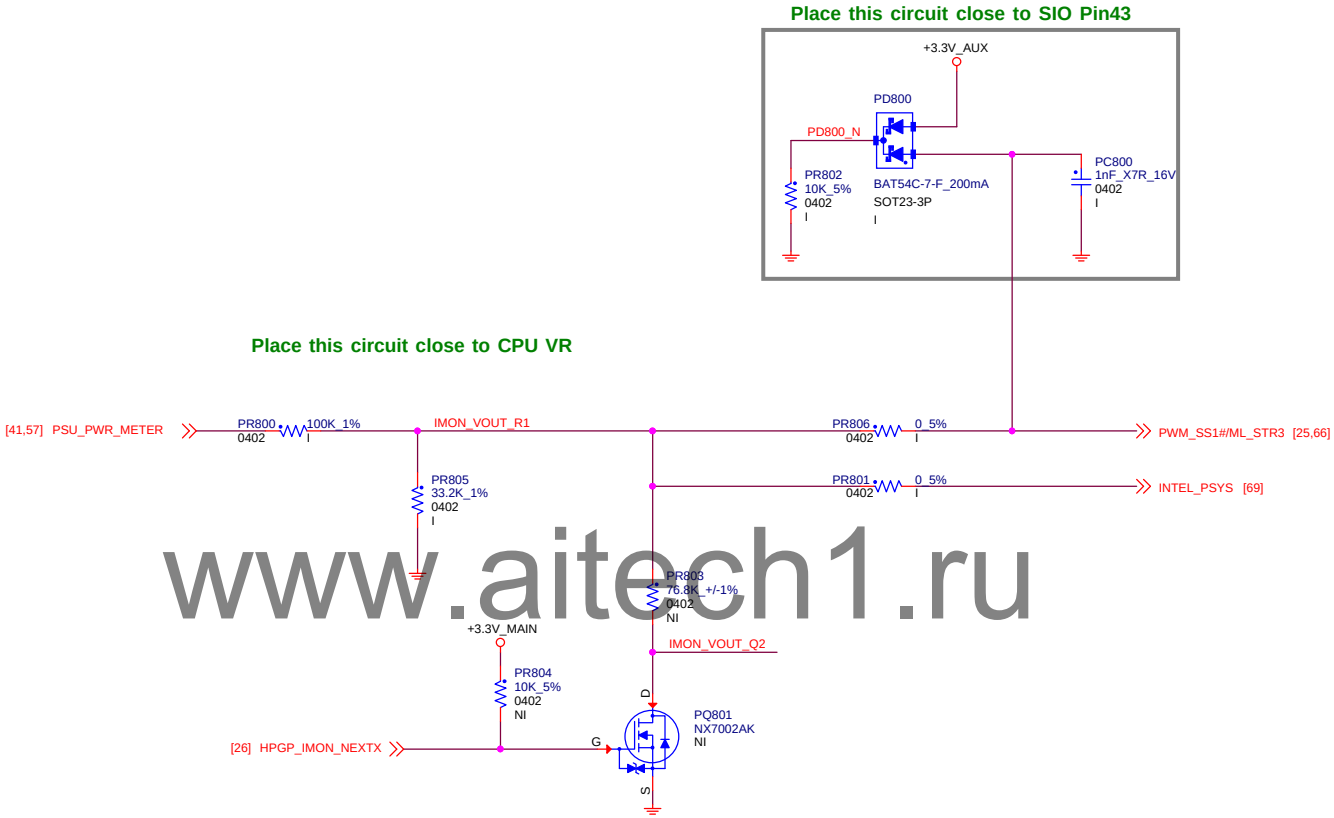
Title: D8_CLINK Header

Size	Document Number	Rev
A	901015-000	A

Date: Wednesday, November 09, 2016 | Sheet 54 of 92

Input Current Monitor



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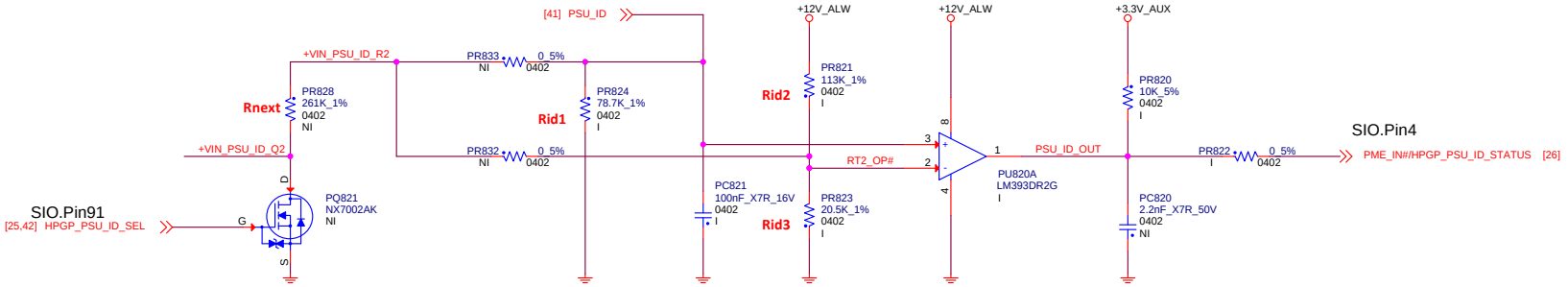
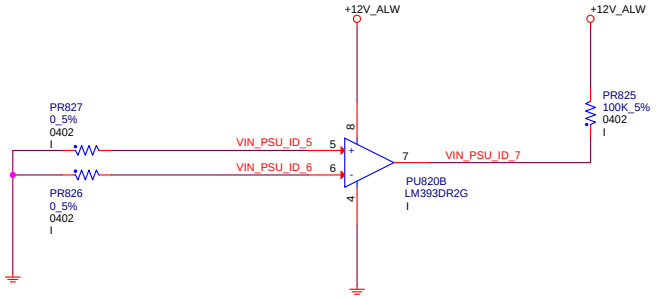
Title	Input Current Monitor	
Custom	795207-000	
Size	Document Number Wednesday, November 09, 2016	Rev A
Date:	Sheet 55 of 92	

Input PSU ID





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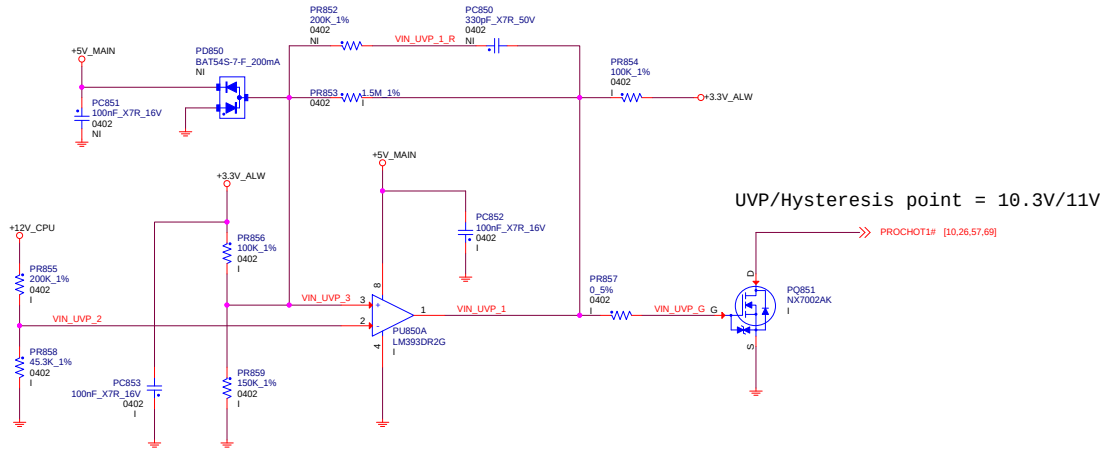
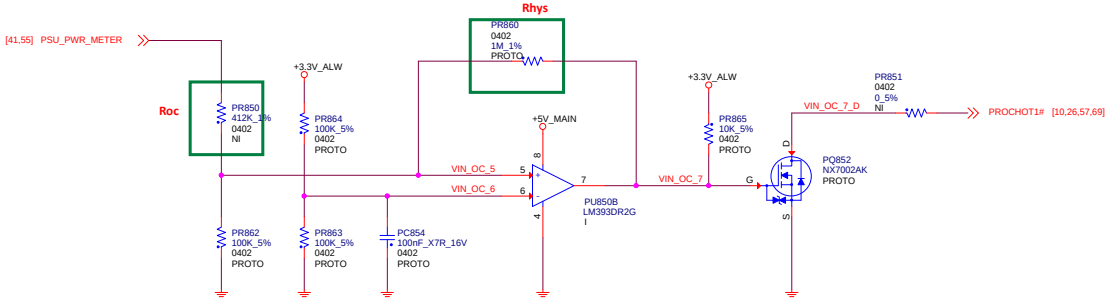
Title	Input PSU ID	
Custom	901015-000	
Size	Document Number Wednesday, November 09, 2016	Rev A
Date:	Sheet 56 of 92	

UVP Throttling



UVP/Hysteresis point = 10.3V/11V

Over-current circuit



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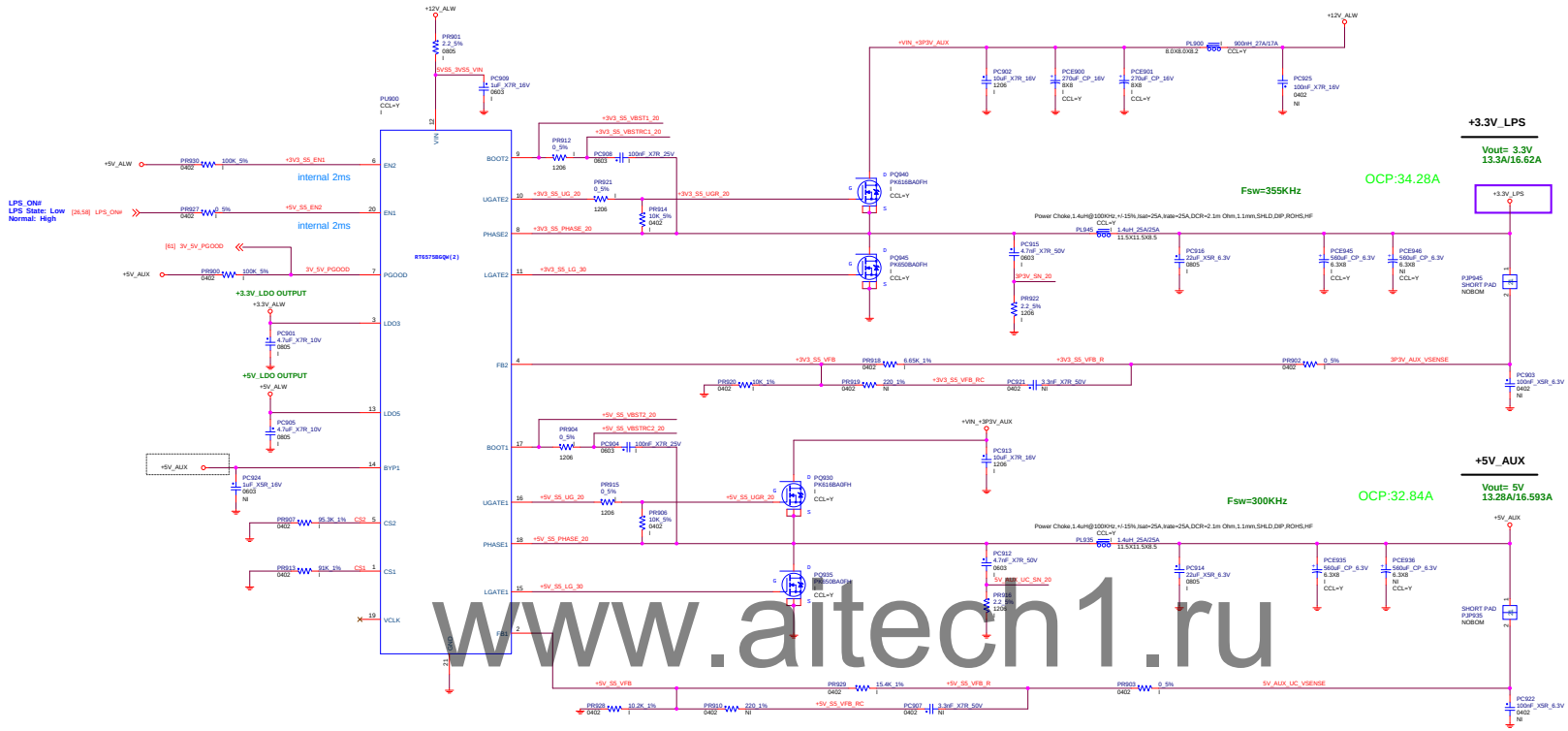
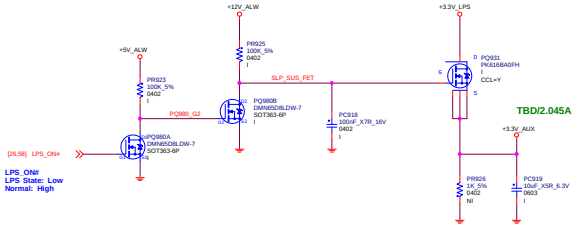
Title	UVP Throttling	
C	901015-000	
Size	Document Number	Rev
	Wednesday, November 09, 2016	A
Date:	Sheet 57 of 92	

System Power





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title	System Power
Size / Custom	Document Number 795367-000
Rev	A
Date: Wednesday, November 09, 2016	Sheet 58 of 92

+5V_GPIO

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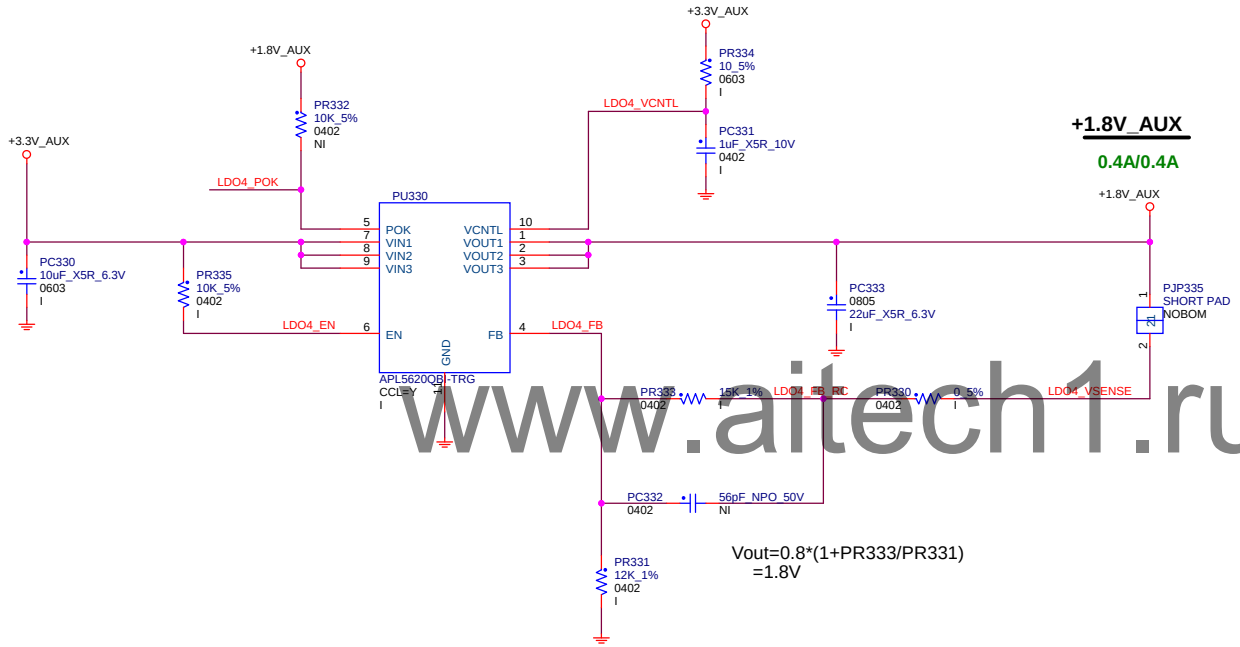
Title	+5V_GPIO	
Size: Custom	Document Number: 901015-000	Rev: A
Date: Wednesday, November 09, 2016	Sheet 59 of 92	

+1.8V_AUX



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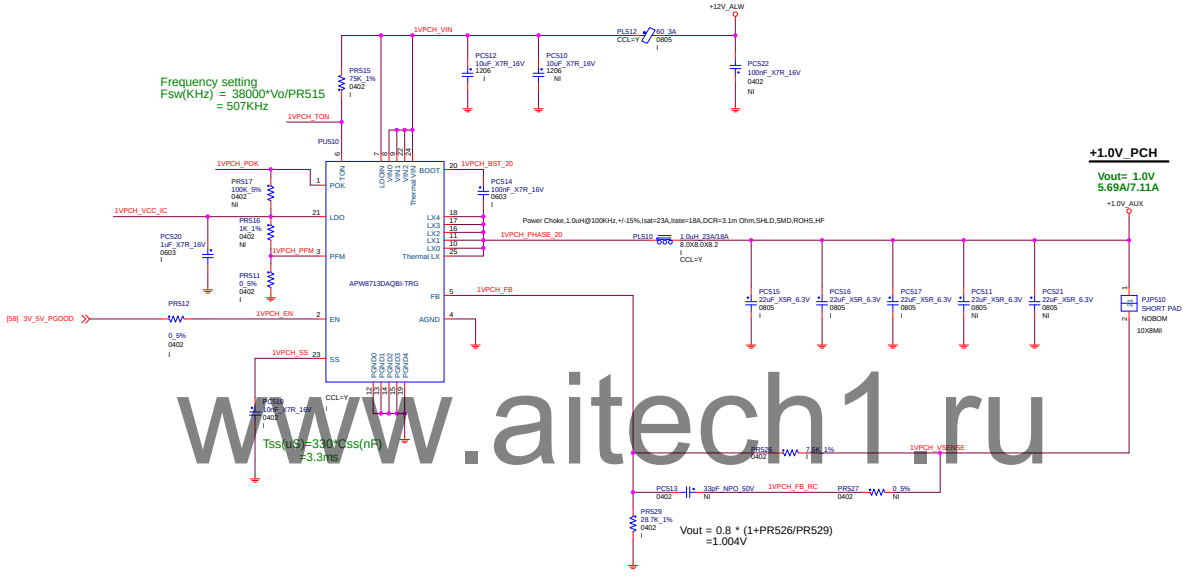
Title +1.8V_AUX

Size Custom | Document Number 901015-000 | Rev A

Date: Wednesday, November 09, 2016 | Sheet 60 of 92

+1.0V_PCH



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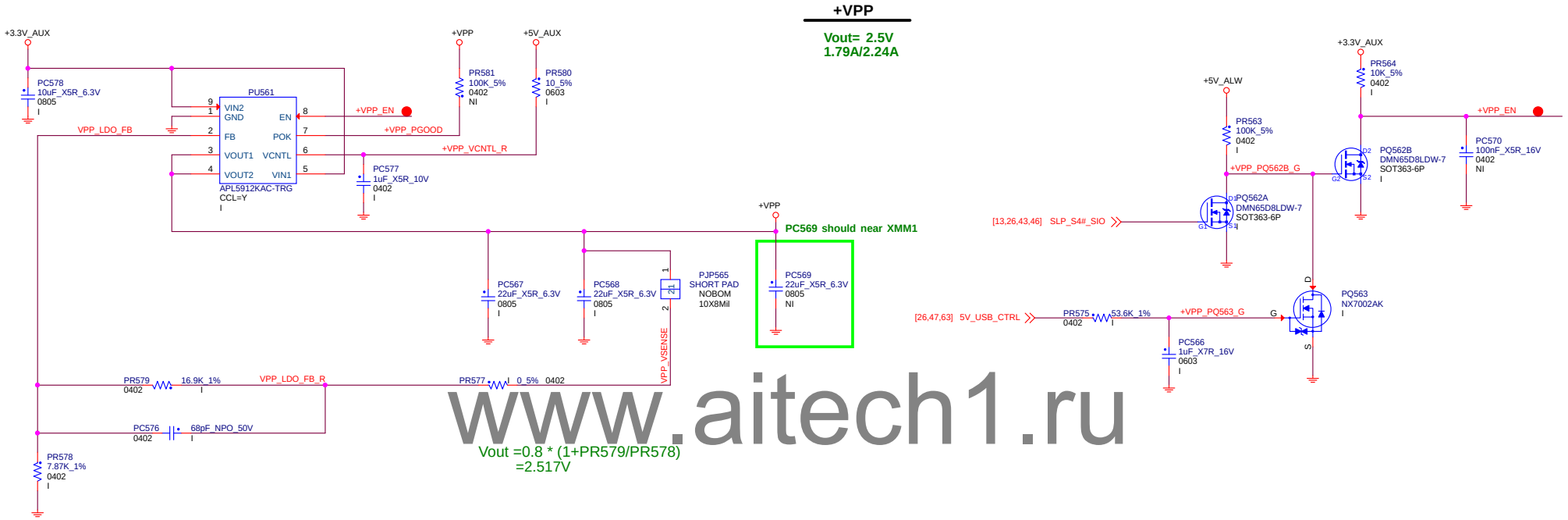
title +1.0V_AUX

Size Document Number Rev
Custom 901015-000 A

Date: Wednesday, November 09, 2016 Sheet 61 of 92

+VPP



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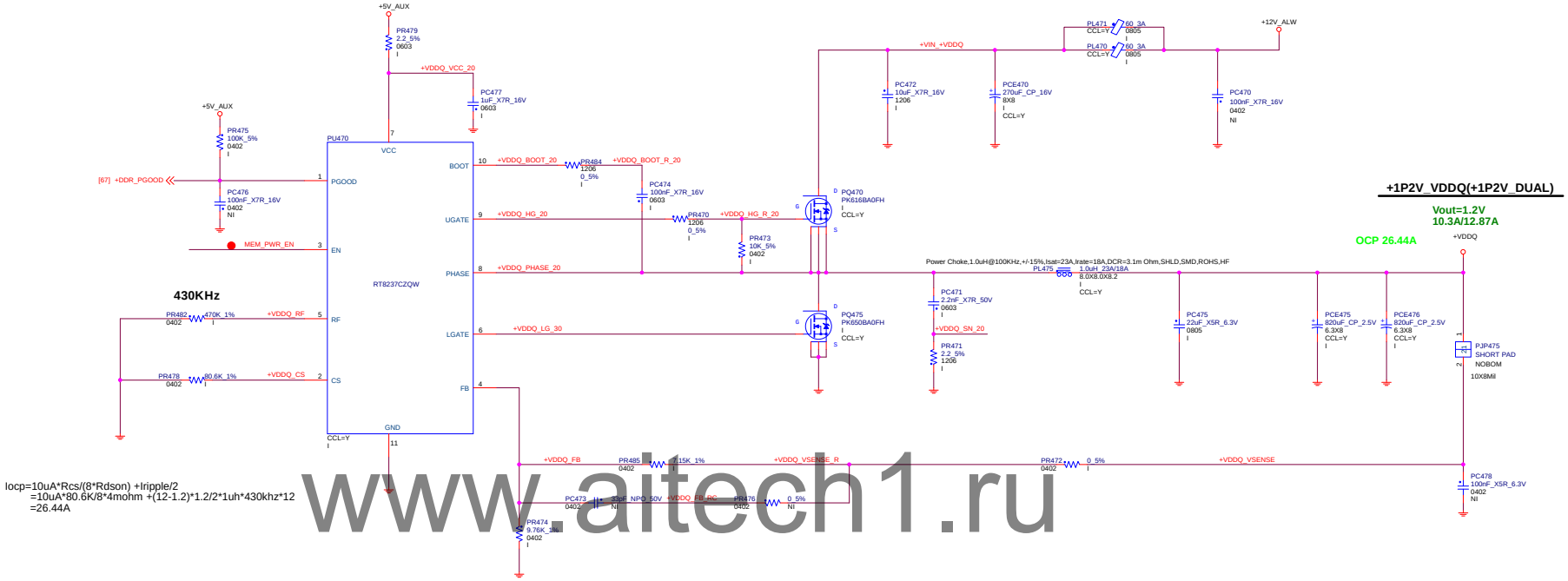
Title +VPP

Size	Document Number	Rev
Custom	901015-000	A

Date: Wednesday, November 09, 2016 Sheet 62 of 92

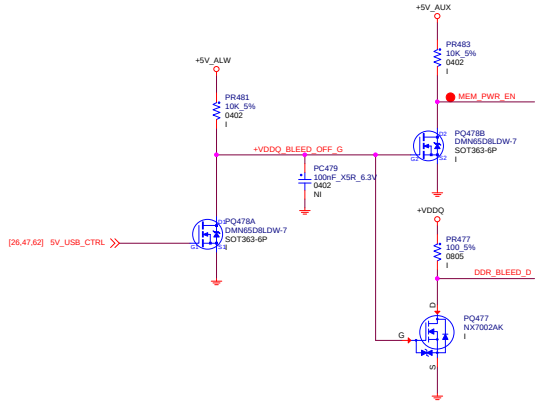
Note: net-name:1P2V_DAUL

+1.2V_VDDQ



Iocp=10uA*Rcs/(8*Rdson) +Iripple/2
=10uA*80.6K/8*4mohm +(12-1.2)*1.2/2*1uh*430khz*12
=26.44A

Vout = 0.704 * (1+PR485/PR474)
=1.207V



+1P2V_VDDQ BLEED OFF

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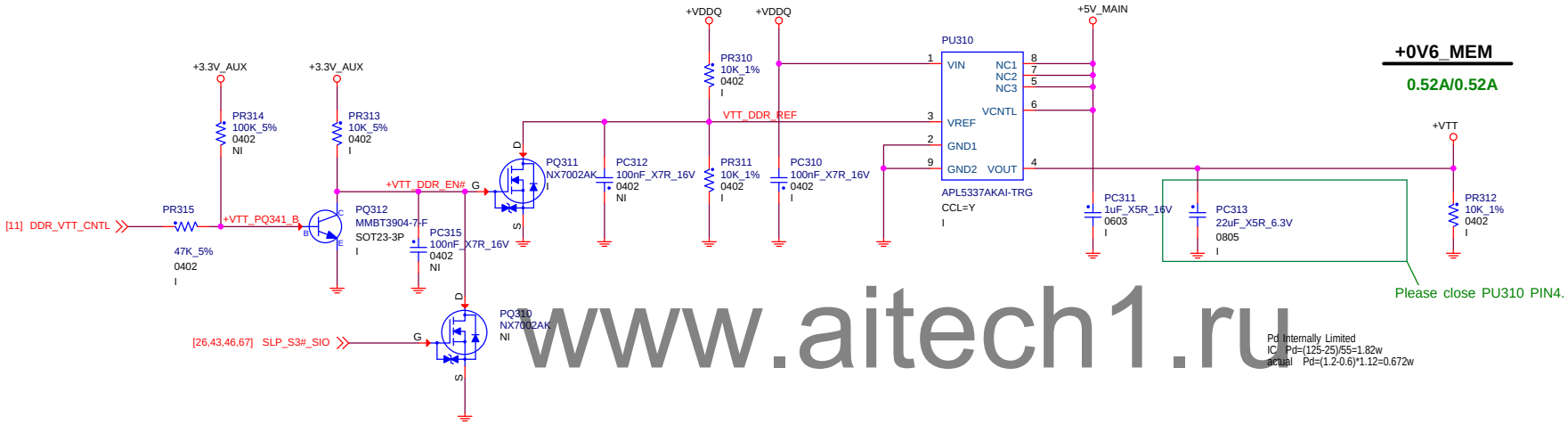
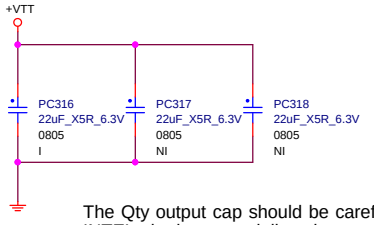
Title	+1P2V_VDDQ
Size	Document Number: Custom 795207-000
Rev	A
Date:	Wednesday, November 09, 2016
Sheet	63 of 92

DDR_VTT



Pd Internally Limited
IC Pd=(125-25)/55=1.82w
actual Pd=(1.2-0.6)*1.12=0.672w



The Qty output cap should be careful
INTEL: the latest modeling shows step load size 6-9x higher than it's shown in PDG 1.0 for Aztec City CRB

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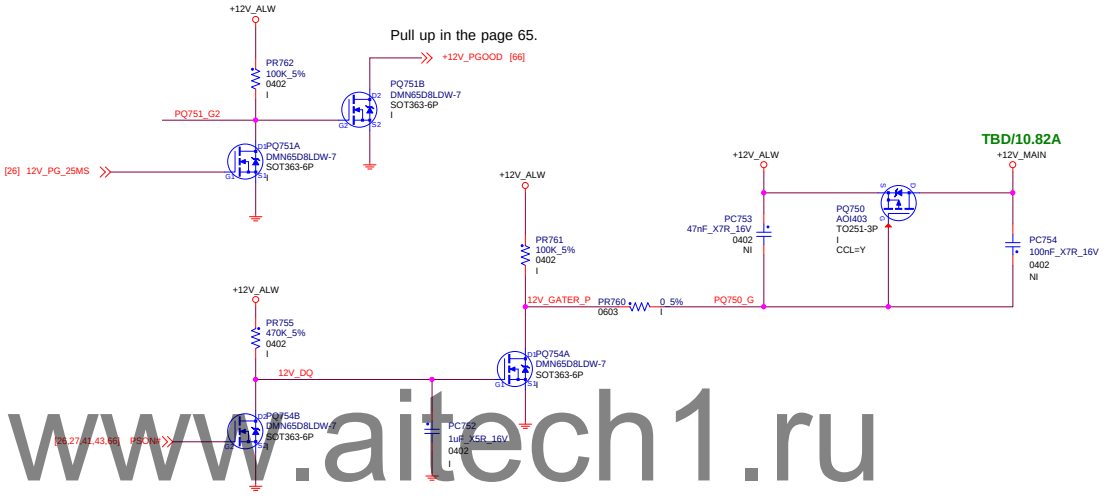
Title +VTT_DDR		
Custom		
Size	Document Number Wednesday, November 09, 2016	Rev A
Date:	Sheet 64 of 92	

+12V



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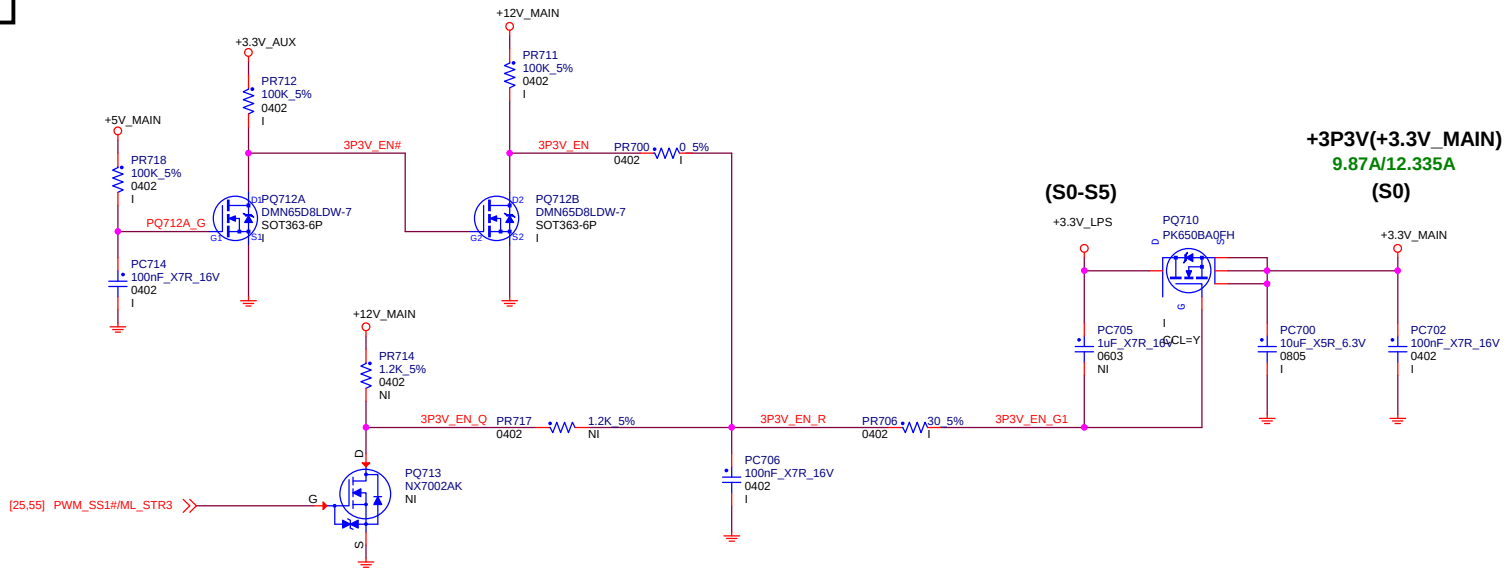
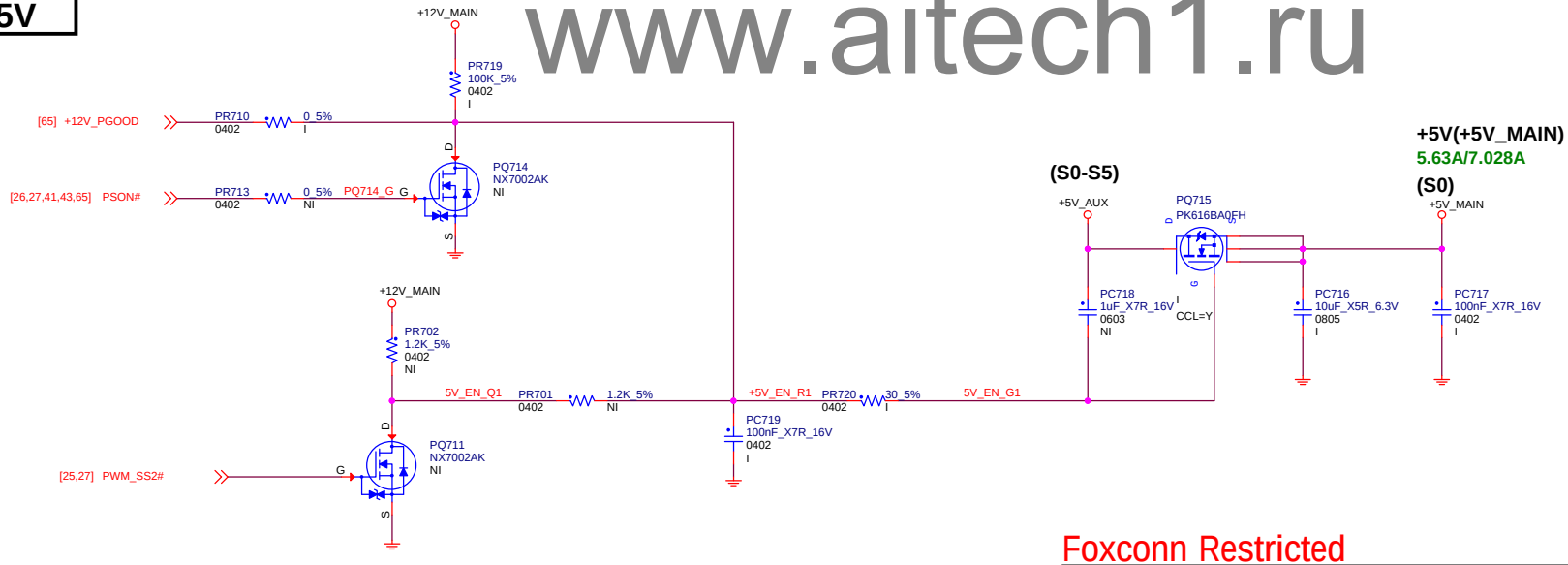
Title	+12V_MAIN	
Size C	Document Number Wednesday, November 09, 2016	Rev A
Date:	Sheet 65 of 92	

+3.3V



+5V



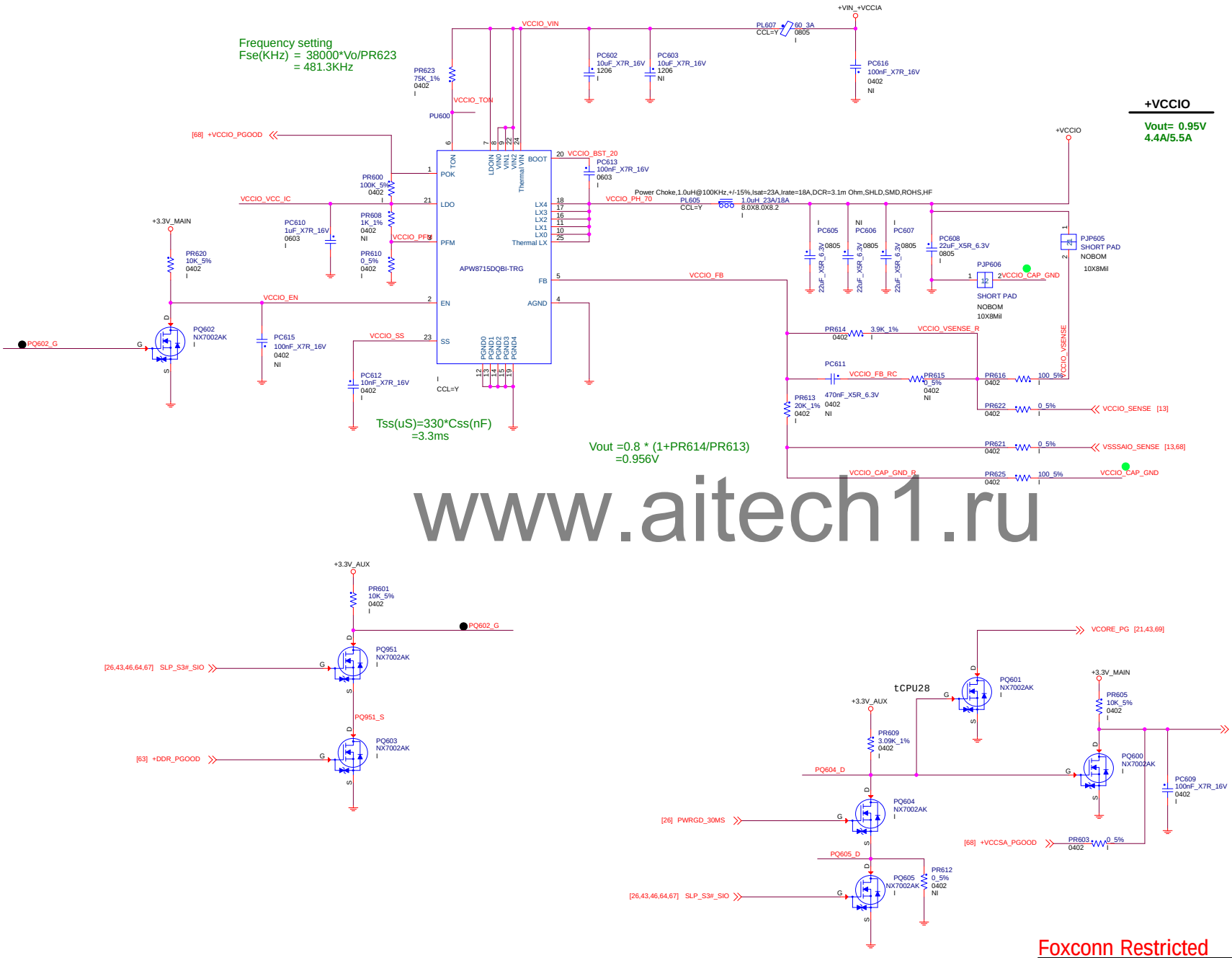
DRAWN BY FOXCONN

Title: +5V_MAIN & +3P3V_MAIN

Size: Custom | Document Number: 901015-000 | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 66 of 92

+VCCIO



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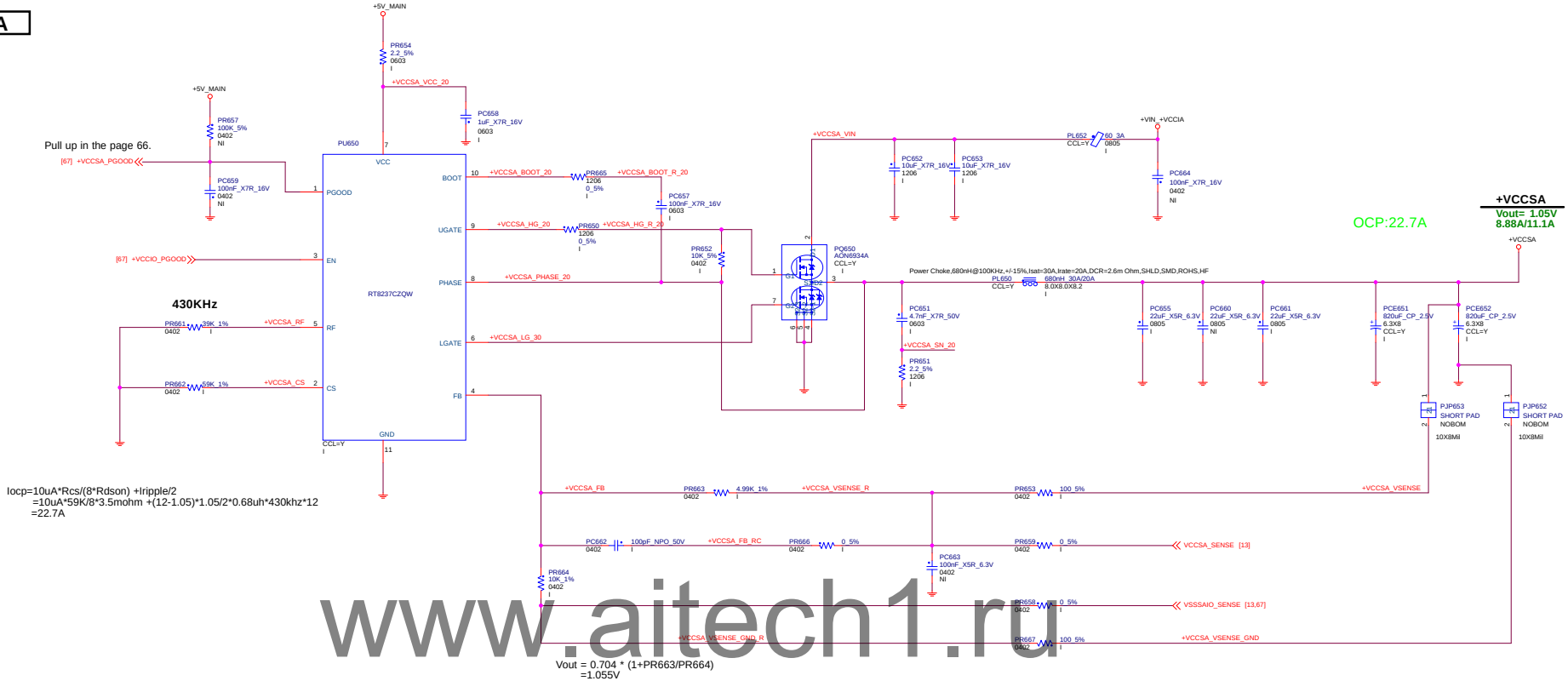
Title	+VCCIO
Size / Document Number	Custom 901015-000
Rev	A
Date: Wednesday, November 09, 2016	Sheet 67 of 92

+VCCSA



Iocp=10uA*Rcs/(8*Rdson) +Iripple/2
=10uA*59K/8*3.5mohm +(12-1.05)*1.05/2*0.68uh*430khz*12
=22.7A

Vout = 0.704 * (1+PR663/PR664)
=1.055V

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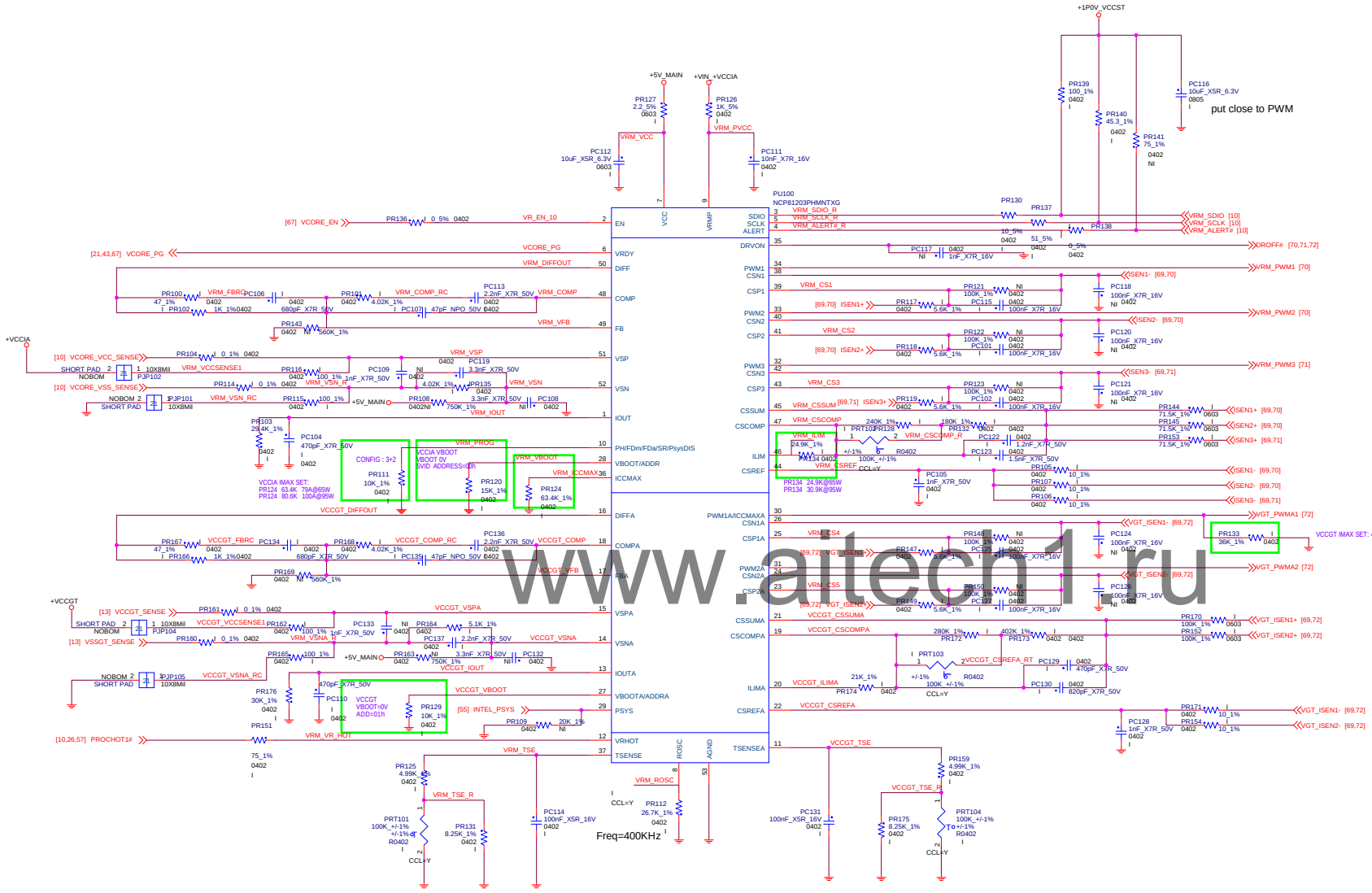
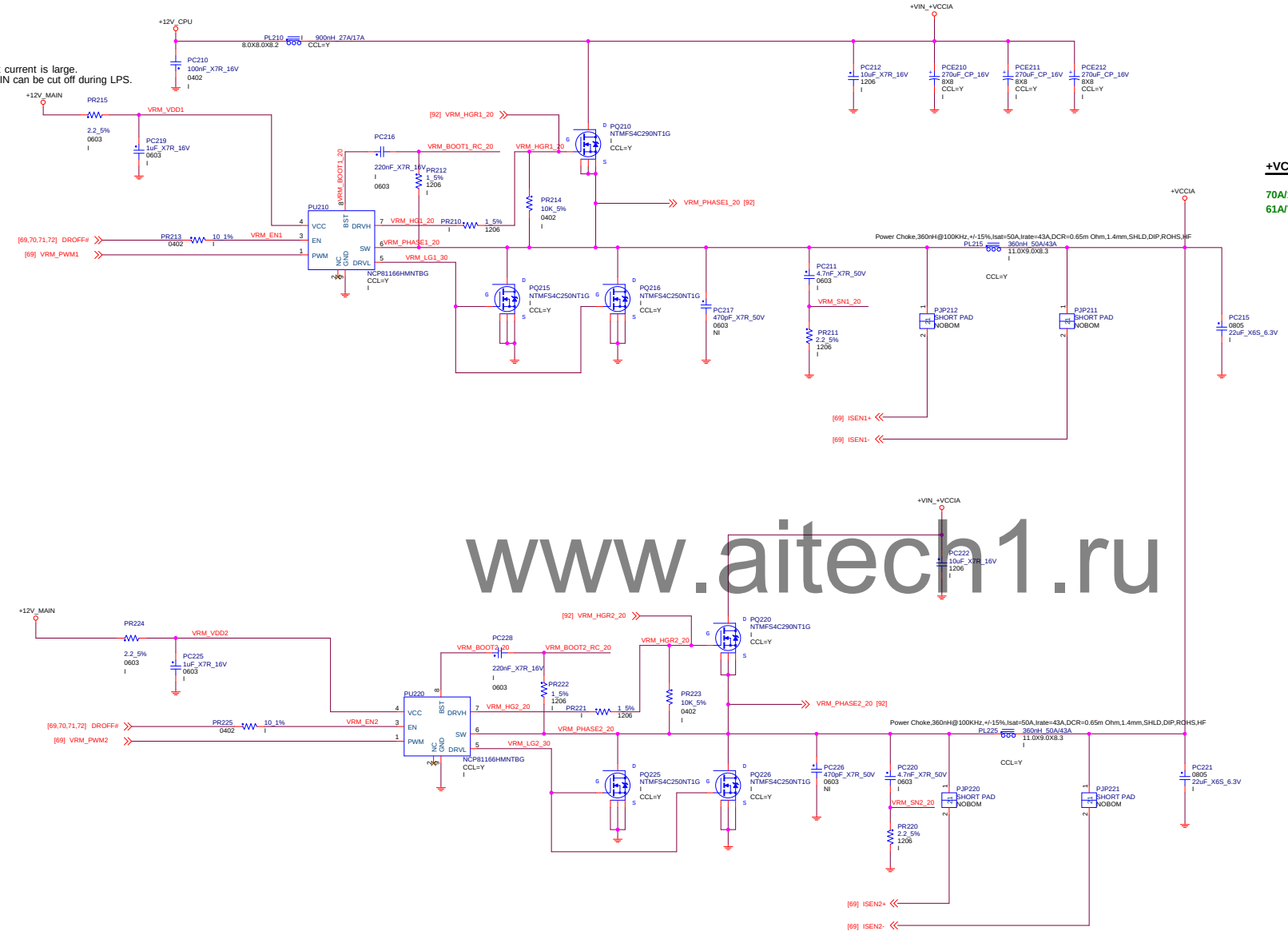
Title	+VCCSA
Size / Document Number / Rev	Custom / 795207-000 / A
Date: Wednesday, November 09, 2016	Sheet 68 of 92



VCORE PHASE1~2

Quiescent current is large.
+12V_MAIN can be cut off during LPS.



+VCCIA

70A/100A 95W
61A/79A 65W

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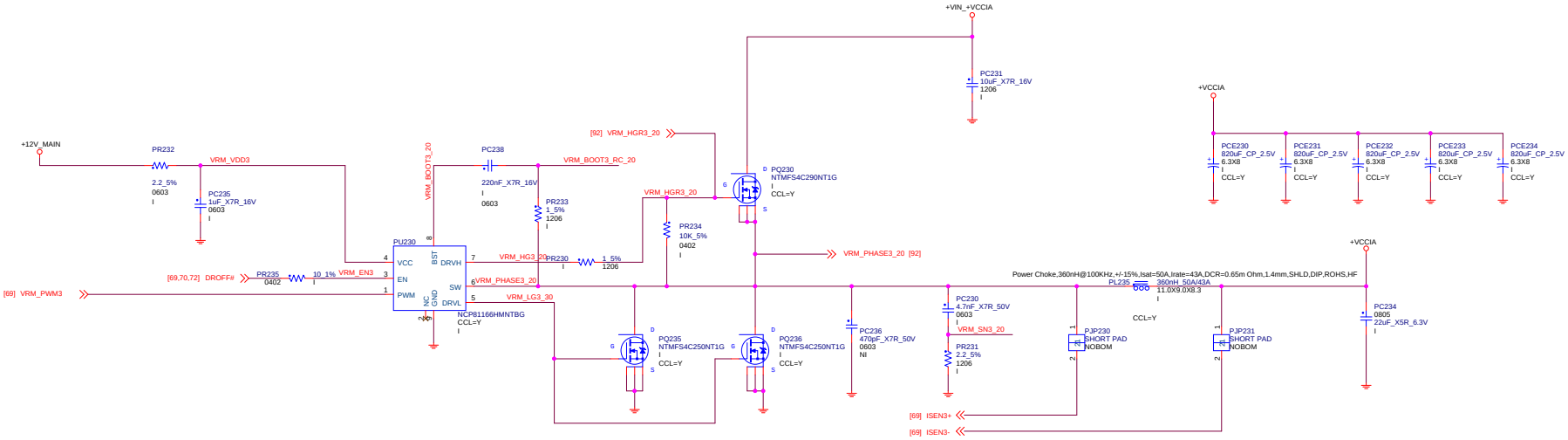
Title	+VCORE PHASE 1 & 2
Size / Document Number	Custom 795207-000
Rev	A
Date:	Wednesday, November 09, 2016
Sheet	70 of 92

VCORE PHASE3



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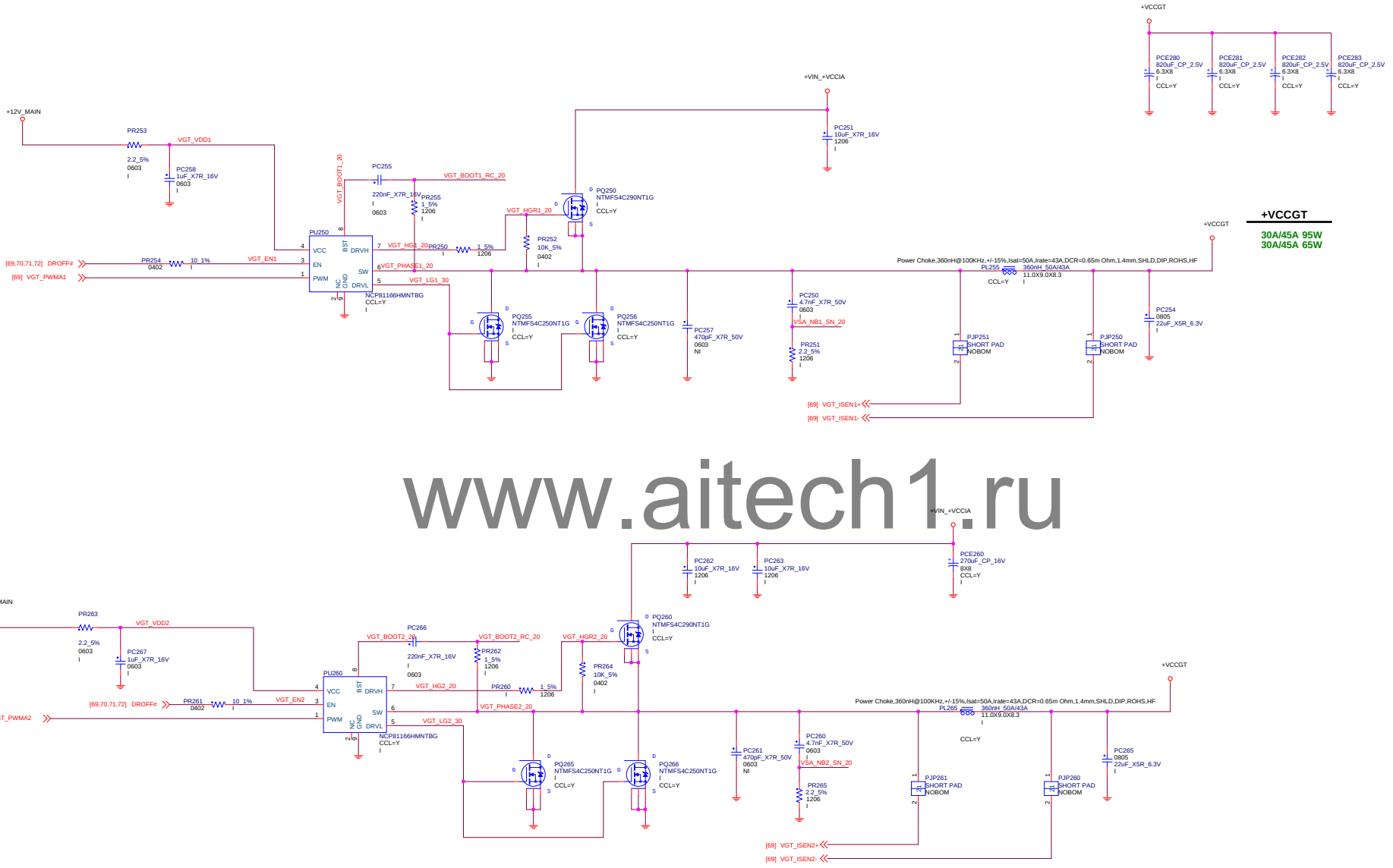
Title +VCORE PHASE 3

Size Custom | Document Number 795207-000 | Rev A

Date: Wednesday, November 09, 2016 | Sheet 71 of 92

VGT PHASE1~2



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Title	+VGT PHASE 1 & 2
Size / Document Number	Custom 795207-000
Rev	A
Date:	Wednesday, November 09, 2016
Sheet	72 of 92

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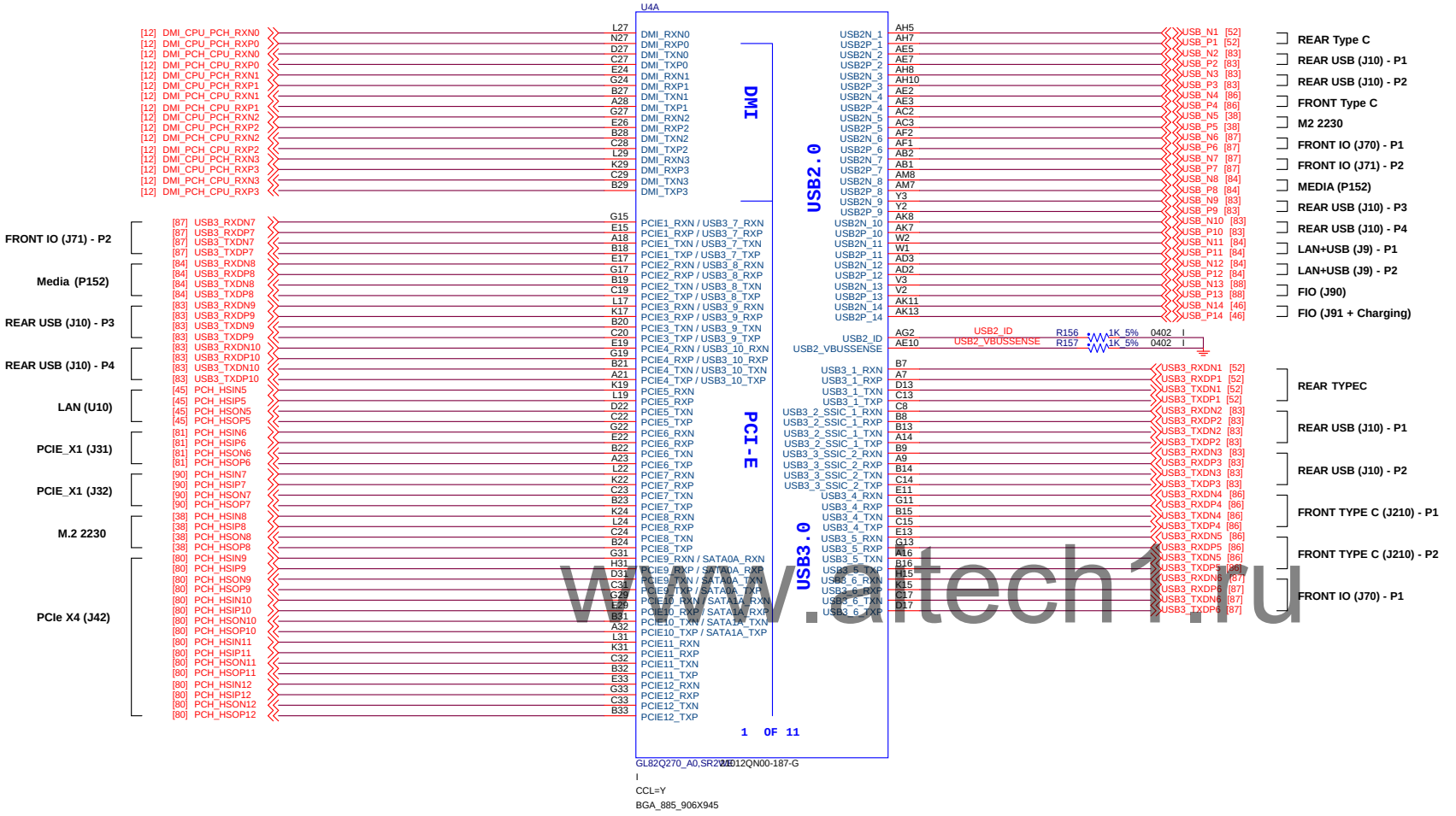
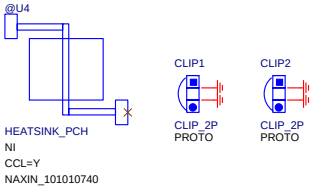
Size: A	Document Number:	Rev: A
Date: Wednesday, November 09, 2016	Sheet 73 of 95	

PCH - DMI/PCIE/USB2-3



PCH HeatSink



Based On HP Port Map - Kabylake201605101530

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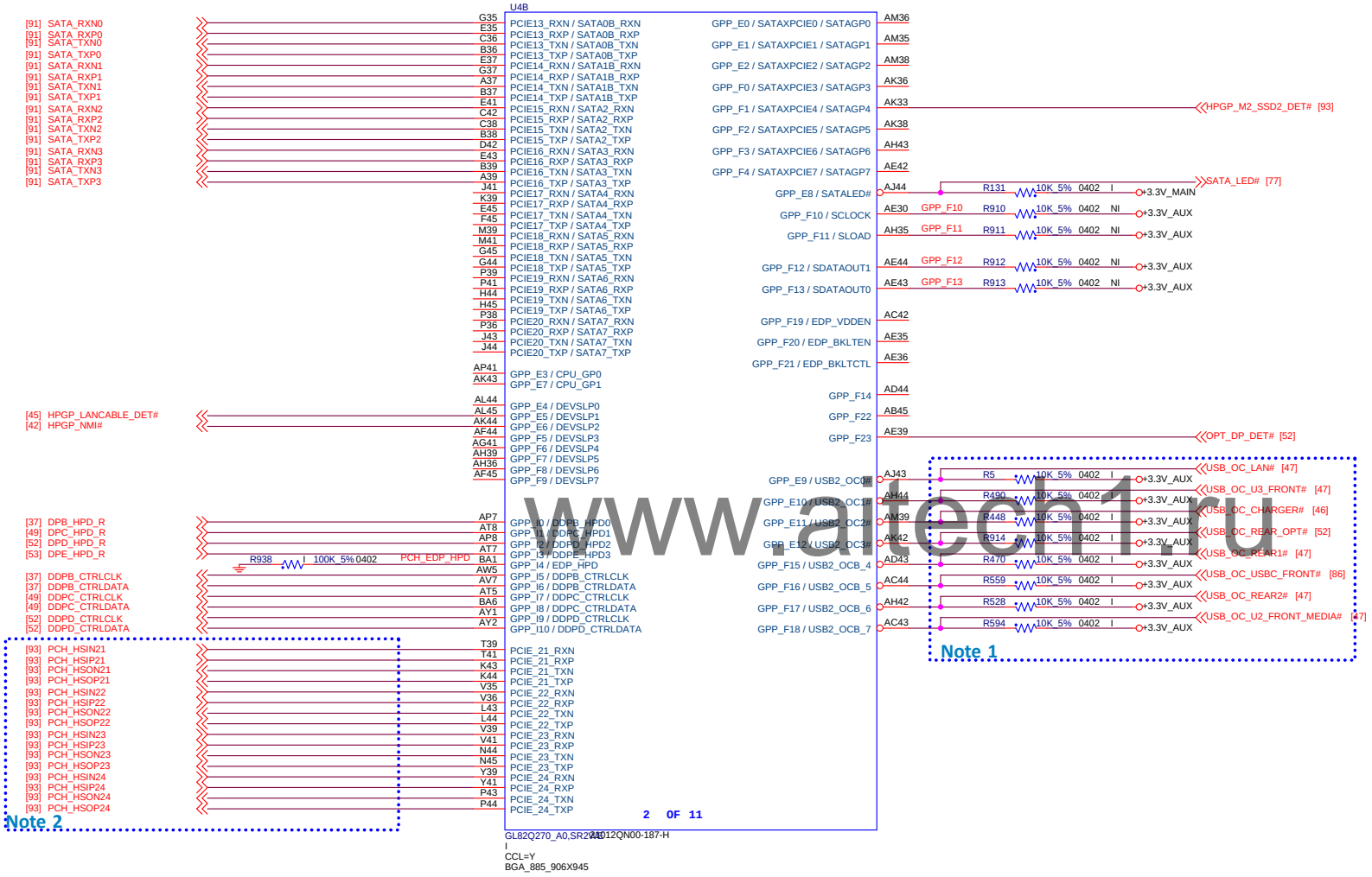
Title: PCH - DMI/PCIE/USB2-3

Size: Custom | Document Number: 901015-000 | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 74 of 95

PCH - SATA/PCIE/HPD/GPIO



Design Note

Note 1

USB2 OC# PORT MAP

OC# MAP config	D8 TWR	D6MT/D8SFF	D4-MT
OC0#	J9	J9	J9
OC1#	P26	J70/J71	J70/J71
OC2#	P24 Charger	J90 Charger	N/A
OC3#	P72	P72	N/A
OC4#	J10-P3/P4	J10-P3/P4	J10-P3/P4
OC5#	P27	J210	N/A
OC6#	J10-P1/P2	J10-P1/P2	J10-P1/P2
OC7#	P24 Common P152	J91 P152	P150

Note 2

M.2 SSD Card support on Andormeda is PCIe Port 21-24
M.2 SSD Card support on Apus is PCIe Port 17-20
M.2 SSD Card support on Aries is PCIe Port 17-20
M.2 SSD Card support on Auriga is PCIe Port 17-20

Based On HP Port Map - Kabylake201605101530

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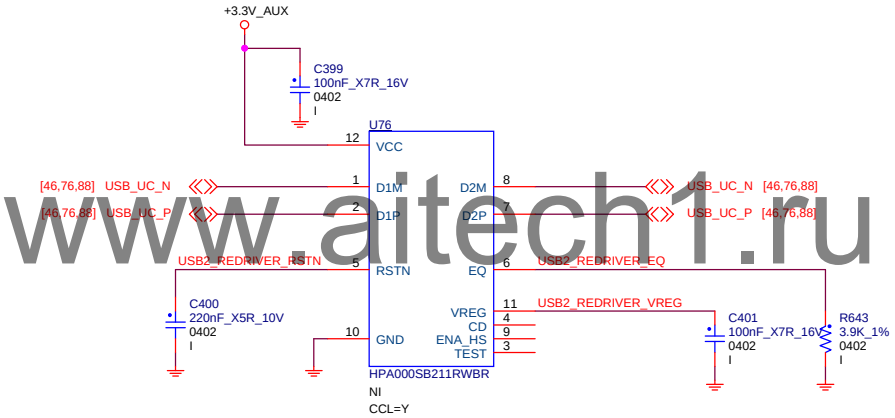
Title: PCH - SATA/PCIE/HPD/GPIO

Size: Custom | Document Number: 901015-000 | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 75 of 95



D1P MUST BE SHORTPAD TO D2P
P1M MUST BE SHORTPAD TO D2M

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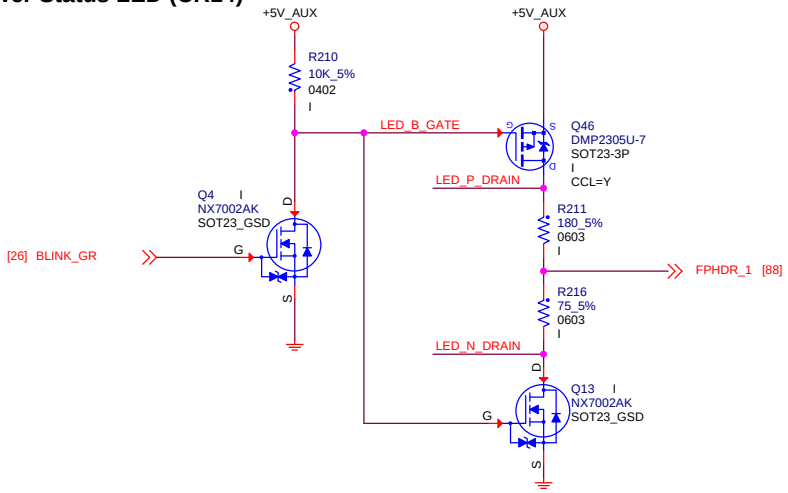
Title
F-USB2-REDRIVER-COMMON

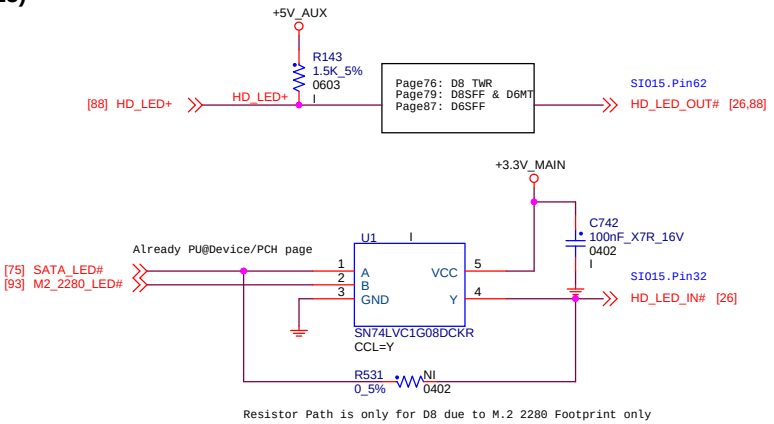
Size	Document Number	Rev
Custom		A

Date: Wednesday, November 09, 2016 | Sheet 76 of 95

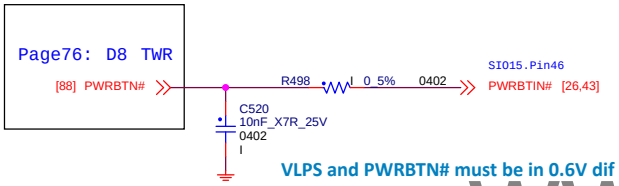
Power Status LED (CR14)



HDD LED (CR15)



Power Button

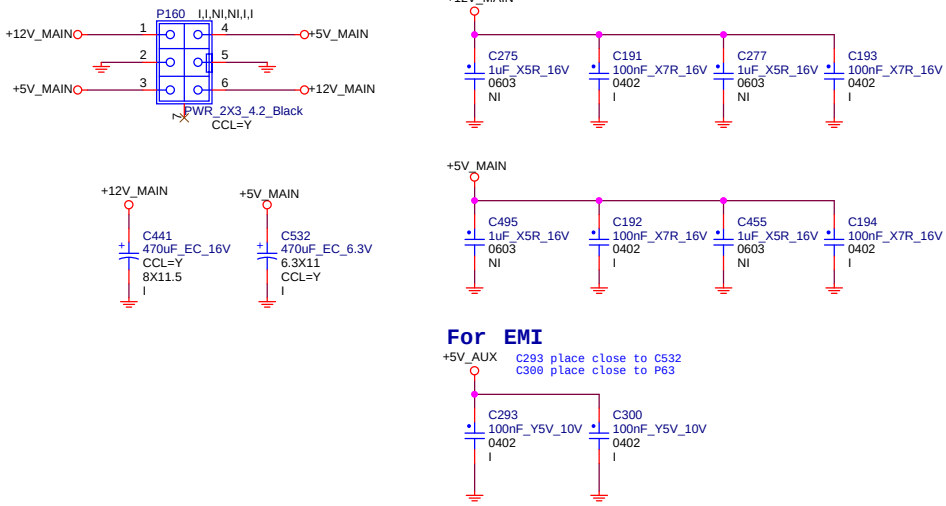


VLPS and PWRBTN# must be in 0.6V dif f erence

SIO_BEEP

Move to CODEC Page for core design leverage

SATA POWER



For EMI

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Size / Document Number	Custom / Rev A
Date: Wednesday, November 09, 2016	Sheet 77 of 95

HD AUDIO CODEC

Design Note

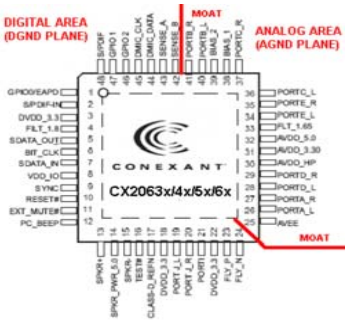
PortABC (Merged Mode): Front Panel CTIA Headset/ HP retask to MIC/LineIn

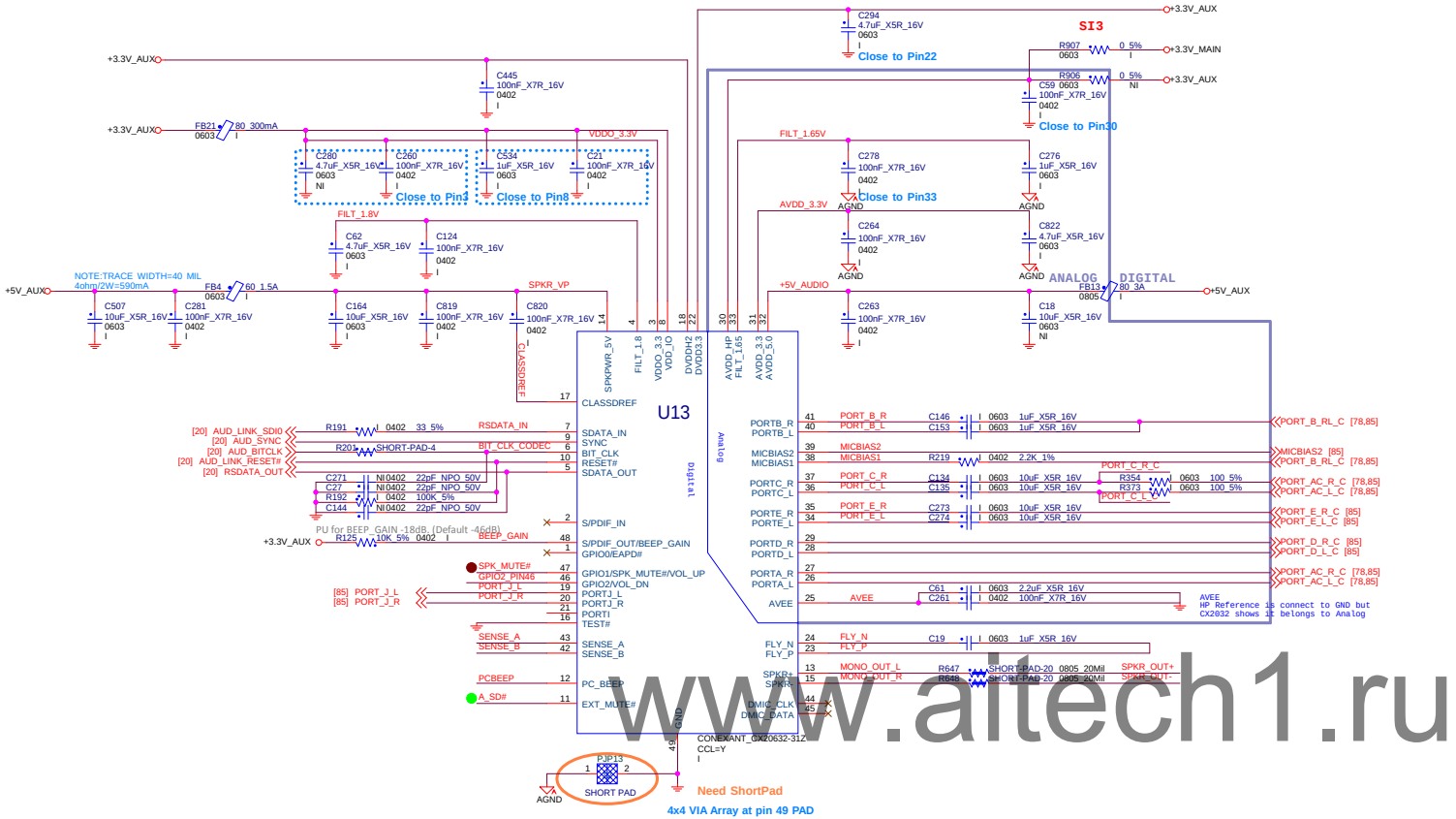
PortD: Front Panel Fix HP

PortJ: Rear LineOut

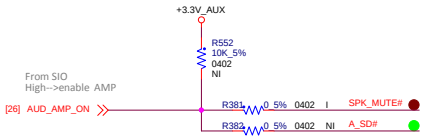
PortE: Rear LineIn (Retask to MIC)

PortG: Mono Class D internal Speaker

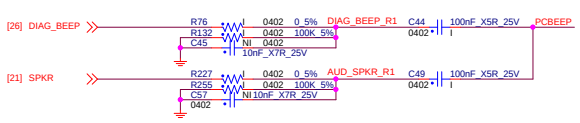




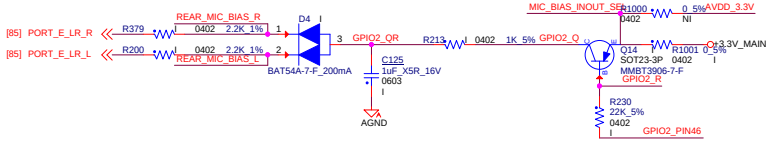
CODEC AMP CONTROL CIRCUIT



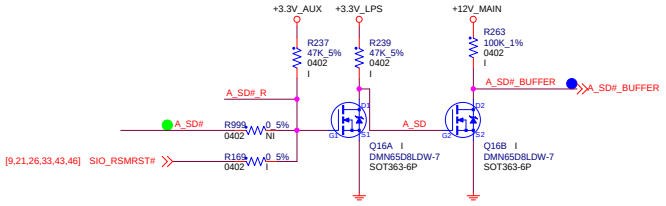
PC BEEP



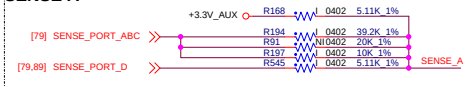
Rear LineIn/MicIn BIAS



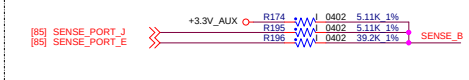
Rear LineOut with Anti-Pop



SENSE A

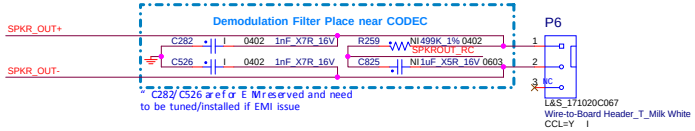


SENSE B



INTERNAL SPEAKER

Speaker 4 Ohm => 20mils (40 mils recommanded)
Speaker 8 Ohm => 10mils (20 mils recommanded)



* C282/C526 are for EMI reserved and need to be tuned/installed if EMI issue

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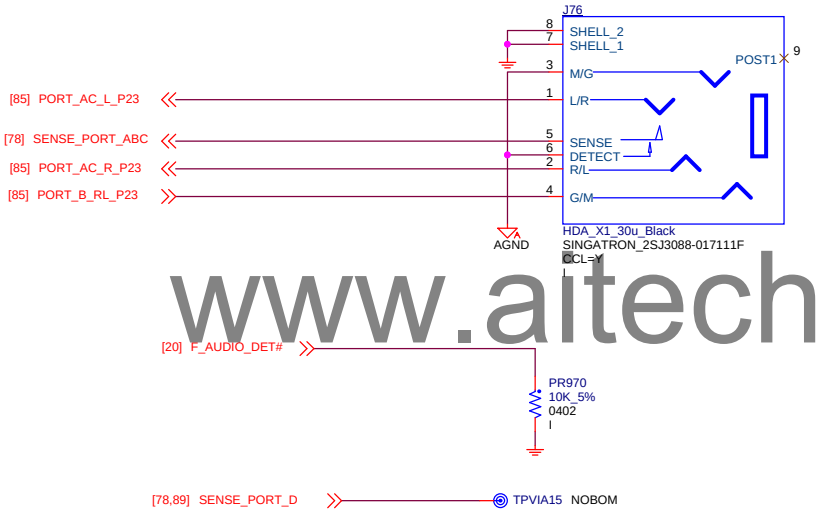
Title	AUDIO CODEC-COMMON-1
Size / Document Number / Rev	A
Date: Wednesday, November 09, 2016	Sheet 78 of 95

CTIA Headset UAJ(Universal Audio Jack)



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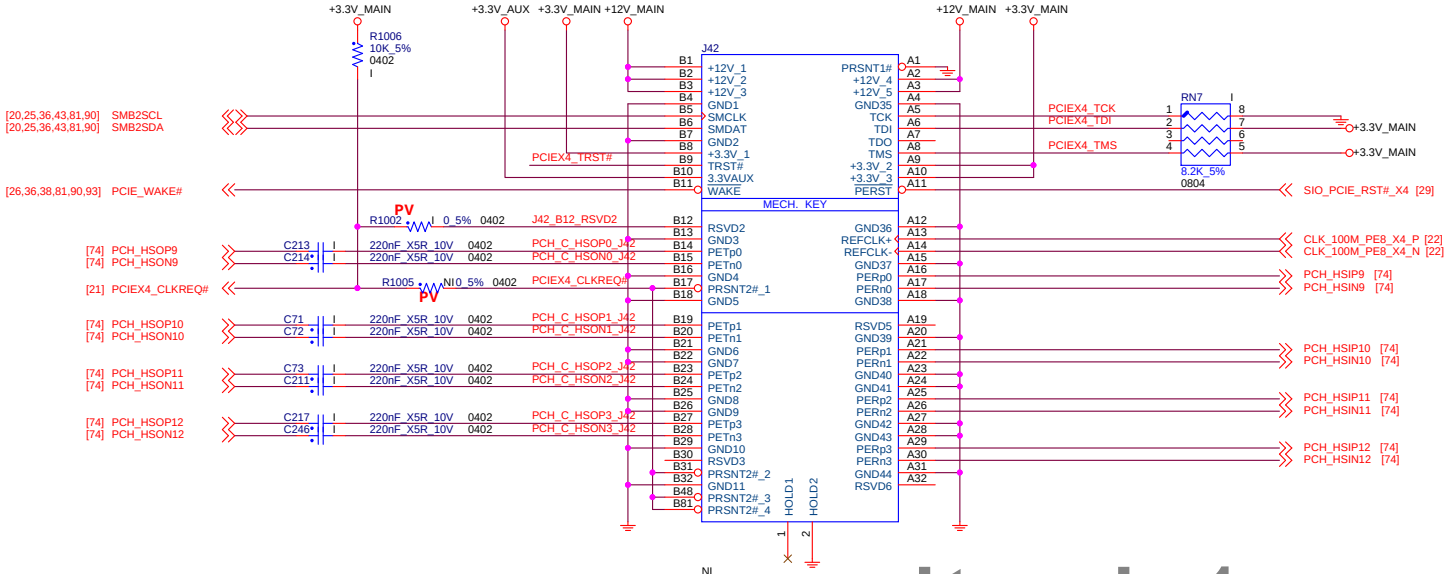
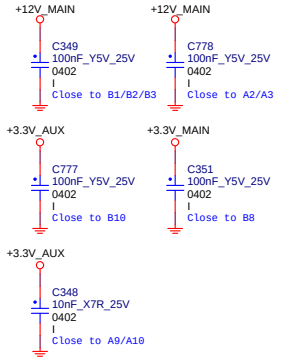
Title: REAR RJ45/USB3.0 x2

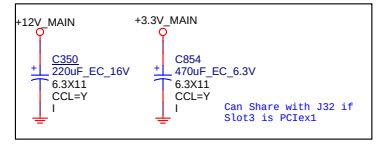
Size	Document Number	Rev
Custom		A

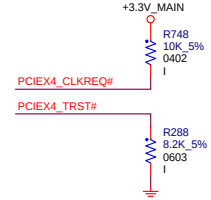
Date: Wednesday, November 09, 2016 | Sheet 79 of 95

PCIe x16 (x4 singal for Optane)

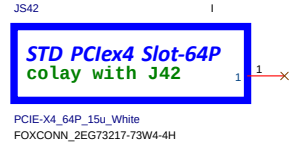








Colay Footprint



Design Note

Note 1
CLKREQ# MUST be connected to X4 Pin B17&B31

Note 2
J42=FOXCONN_2EG73217-73W2-4H, Hold Pin1 is NP, Hold Pin2 is PTH

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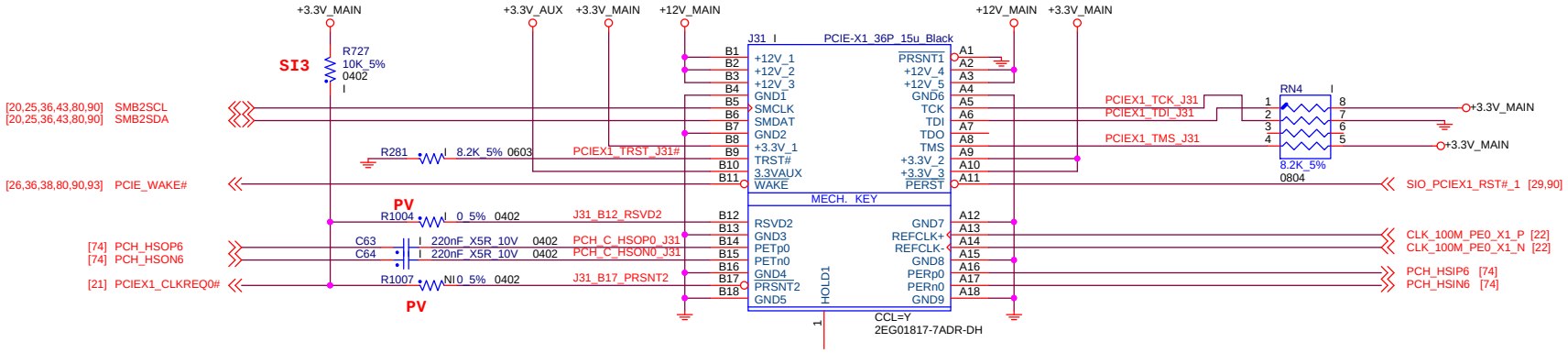
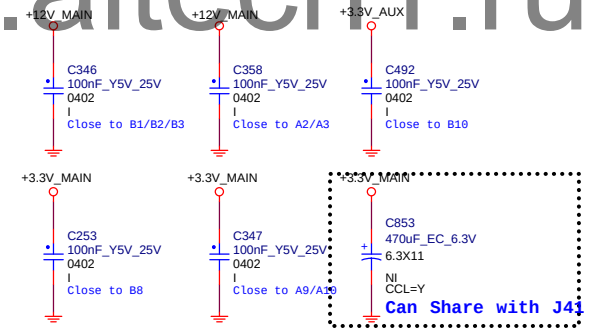
Title	PCIE - x4(SLOT4)-COMMON
Size / Document Number	Custom / Rev A
Date: Wednesday, November 09, 2016	Sheet 80 of 95

PCI EXPRESS X1 SLOT2



PCI EXPRESS X1 SLOT2 Decoupling CAP



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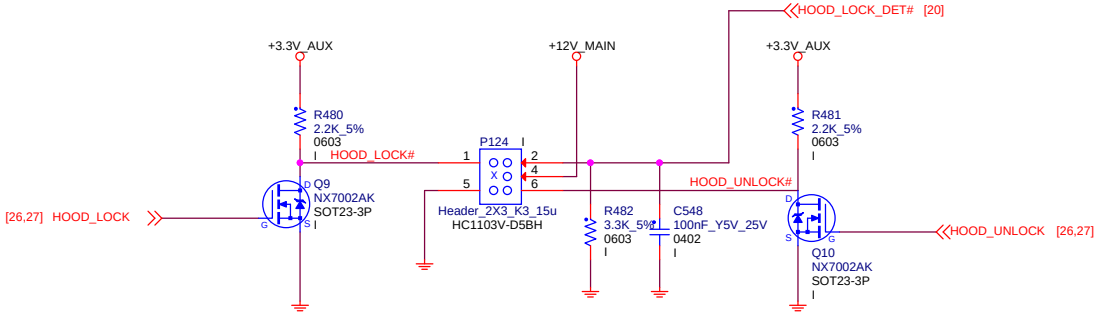
Title: PCIE - x1(SLOT2)-COMMON

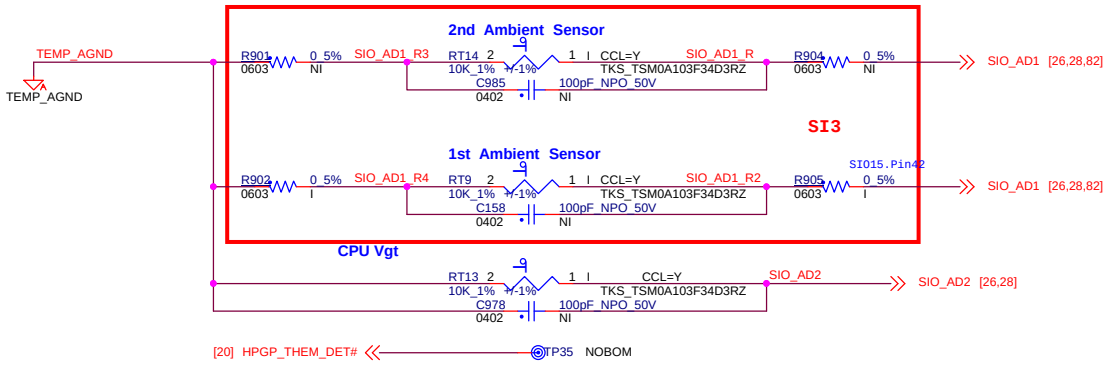
Size: Custom | Document Number | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 81 of 95

HOOD_LOCK



THERMAL SENSORs (SIO15)



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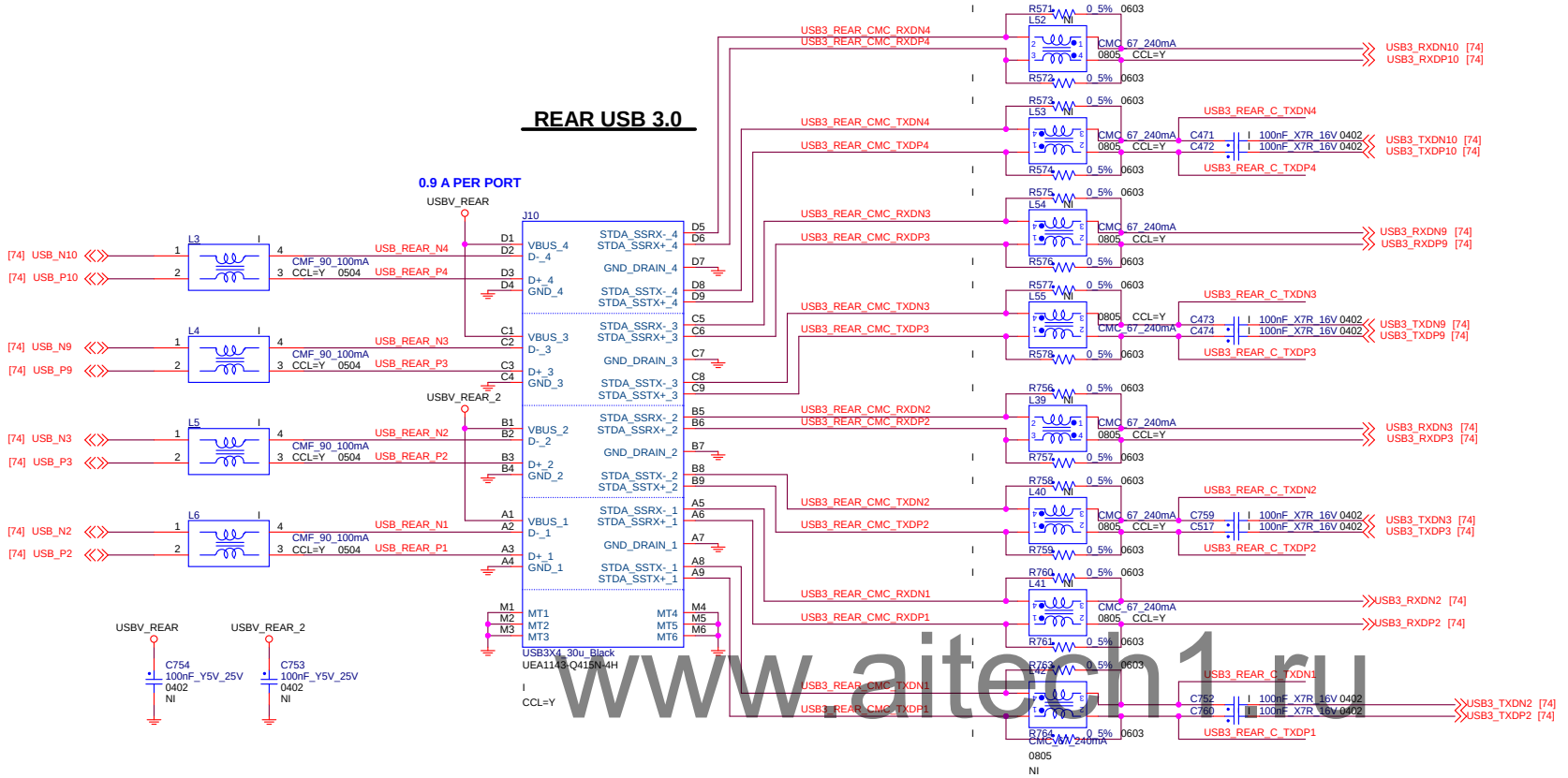
Title: HLOCK-THMAL SENSOR-COMMON

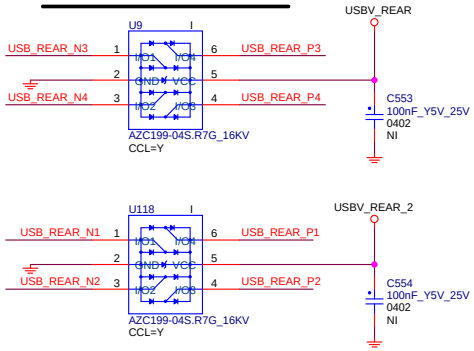
Size: Custom | Document Number | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 82 of 95

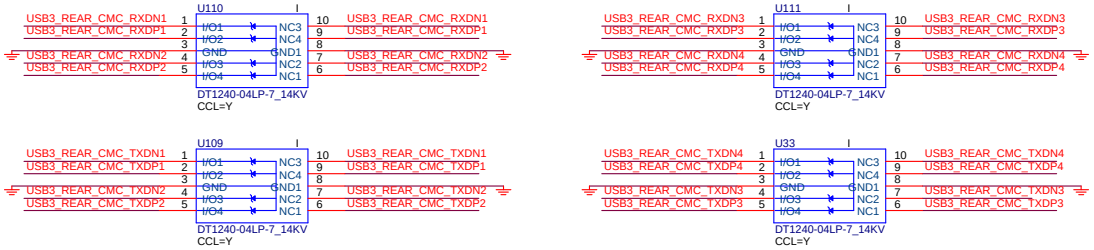
REAR USB 3.0



REAR USB2.0 ESD Component



REAR USB3.0 ESD Component



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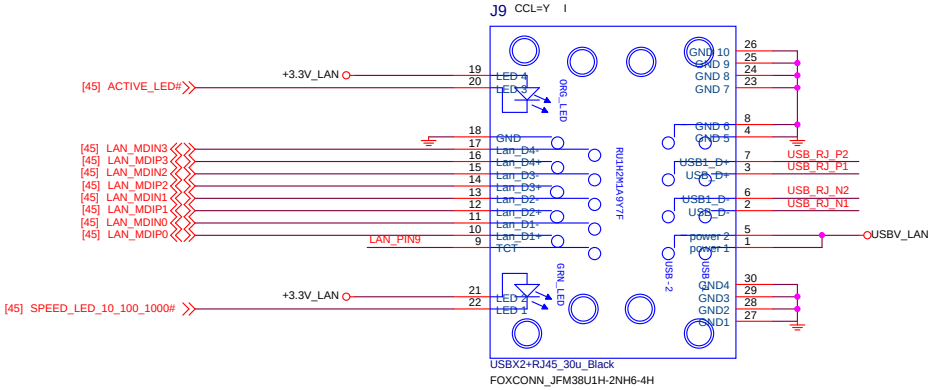
Title: REAR/RJ45/MEDIA USB

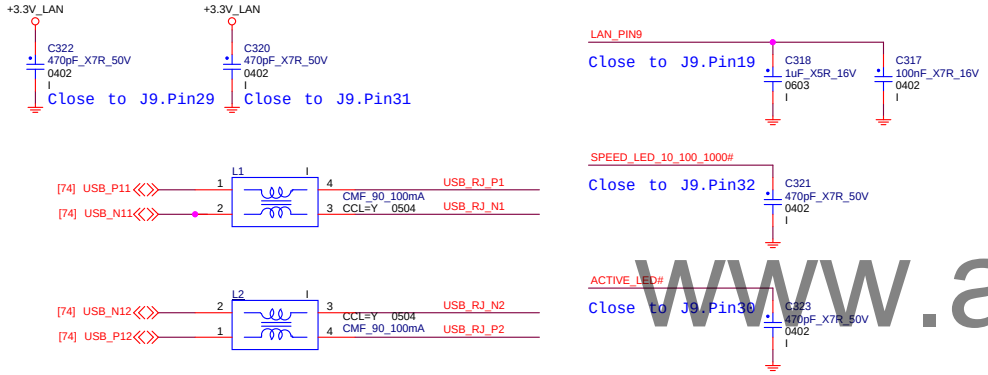
Size: Custom | Document Number | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 83 of 95

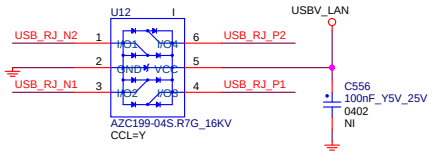
LED's:
10MHz/100MHz:/1GHz : Green
Active LED: Amber

REAR LAN + USB2.0 X2

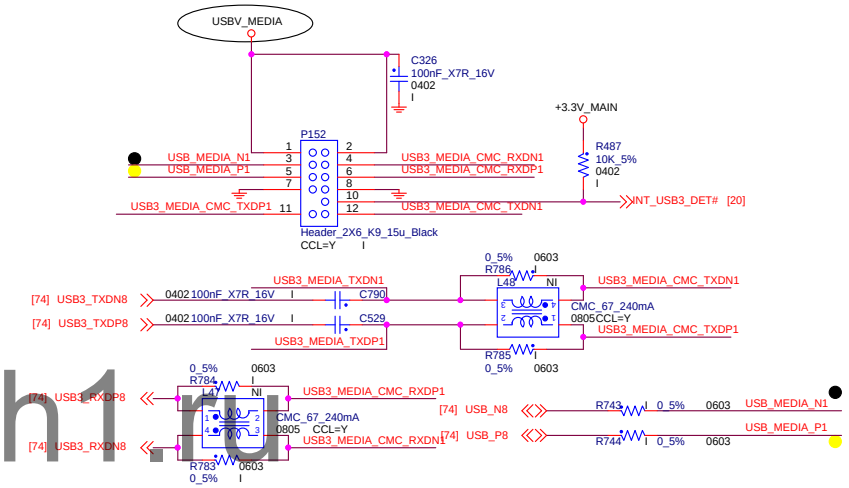




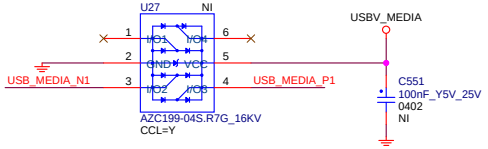
LAN USB ESD Component

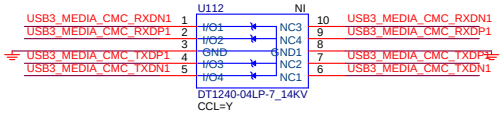


INTERNAL USB3 Header

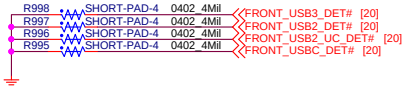


INTERNAL USB3 ESD Component





D8 FIO CABLE TP



Foxconn Restricted Secret

HP RESTRICTED (HP RESTRICTED SECRET)

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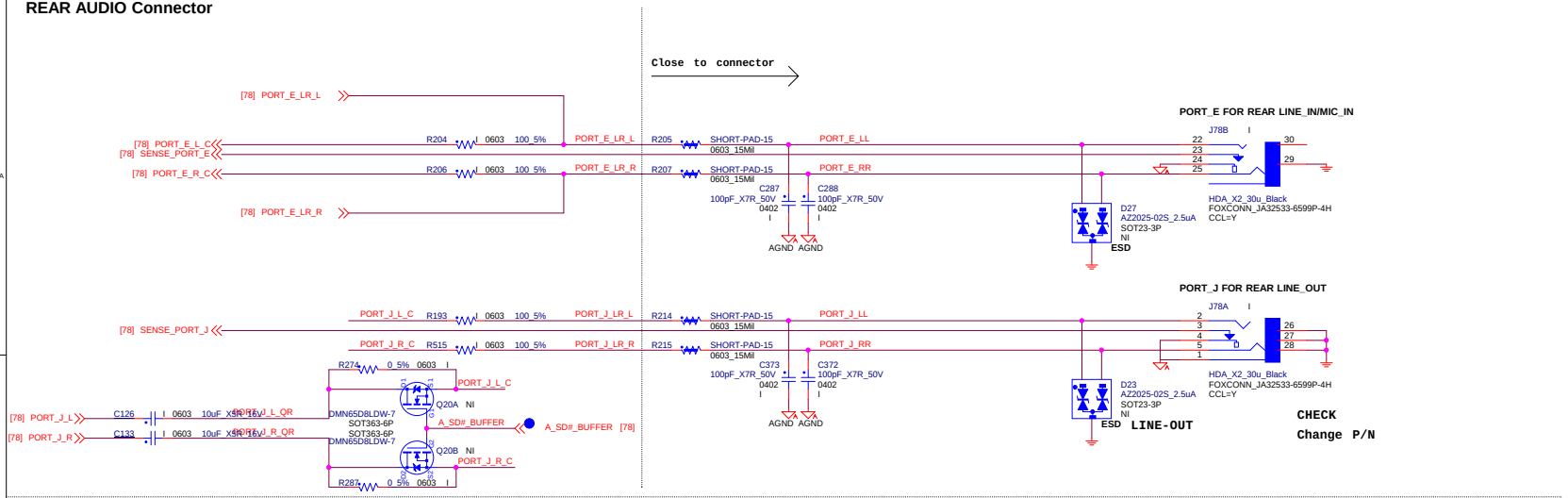
Title: RJ45+USB2/INT-USB3-COMMON

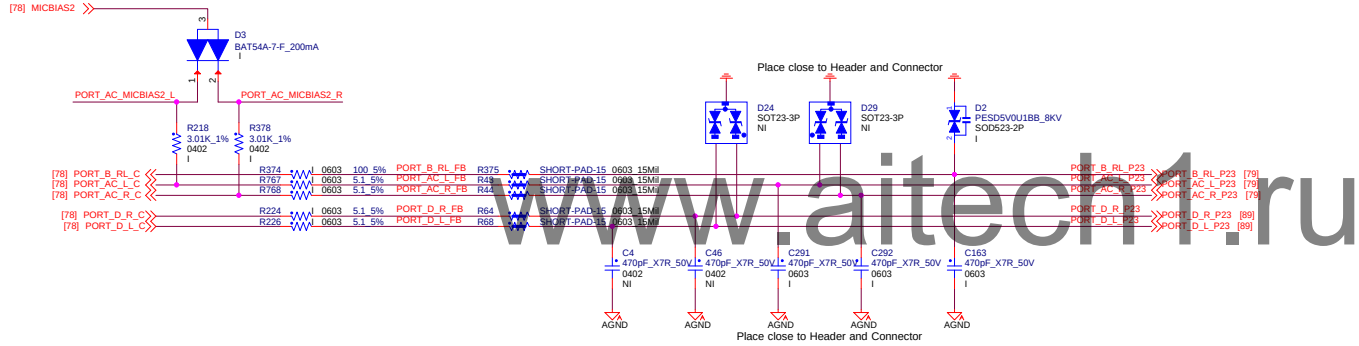
Size: Custom | Document Number | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 84 of 95

REAR AUDIO Connector



FRONT AUDIO HEADER



AUDIO EMI CAP

Foxconn Restricted Secret

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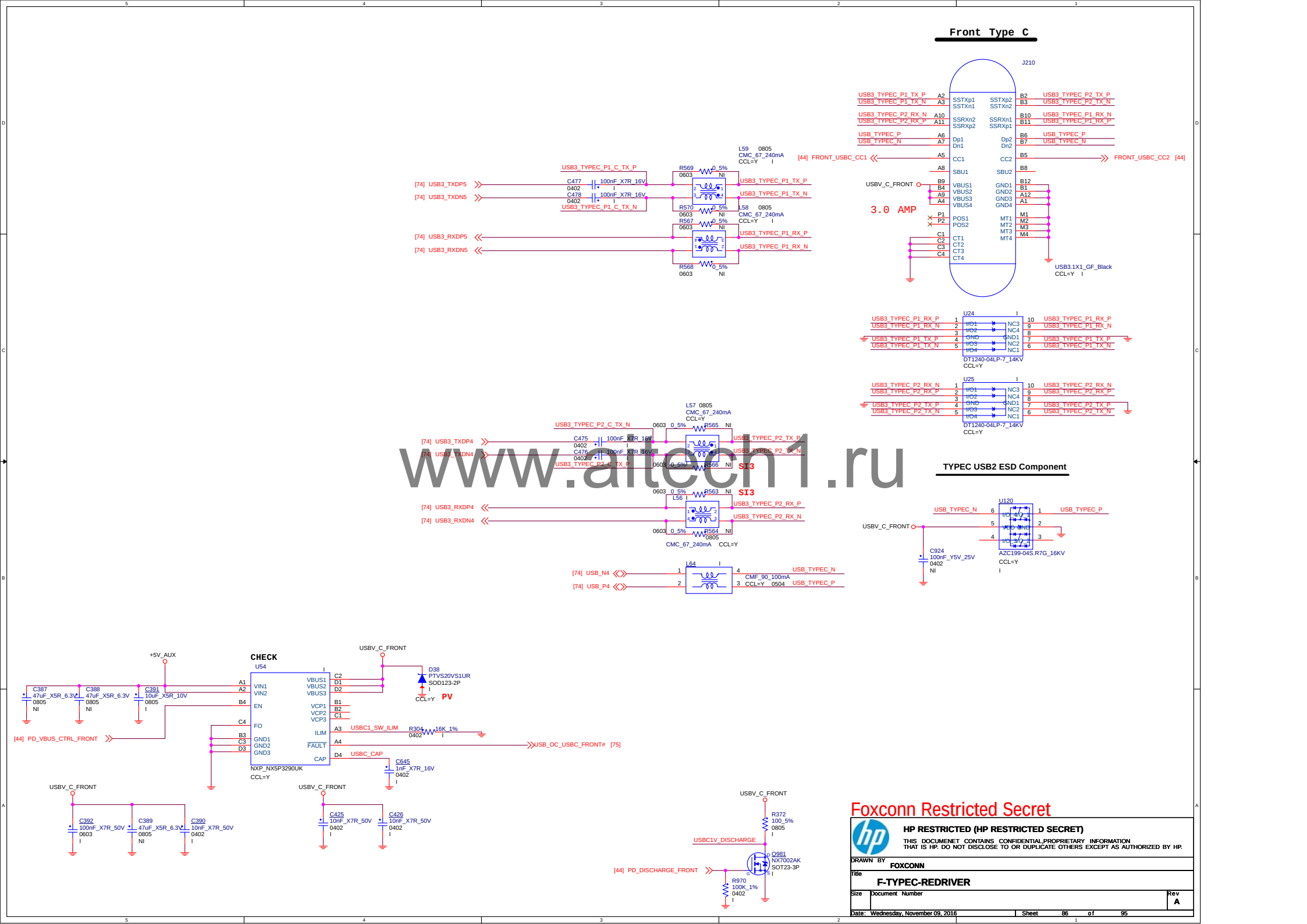
Title: AUDIO CODEC-COMMON-2

Size: Custom | Document Number | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 85 of 95



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Title F-TYPEC-REDRIVER

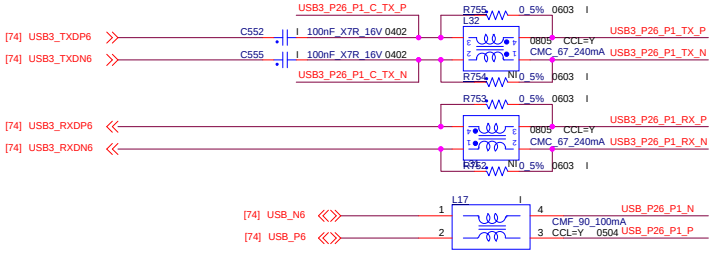
Size | Document Number | Rev A

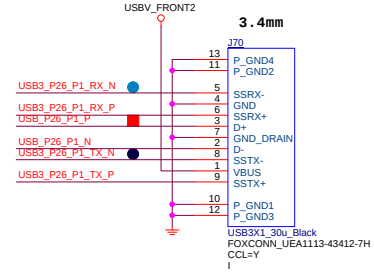
Date: Wednesday, November 09, 2016 | Sheet 86 of 95

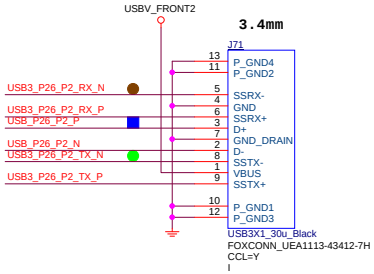
FRONT1 USB 3.0 x 1 (CHARGER PORT)

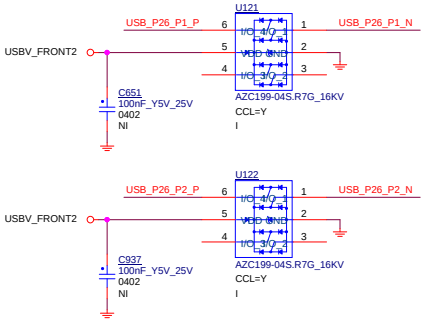
P26 USB 3.0 - Common Parts

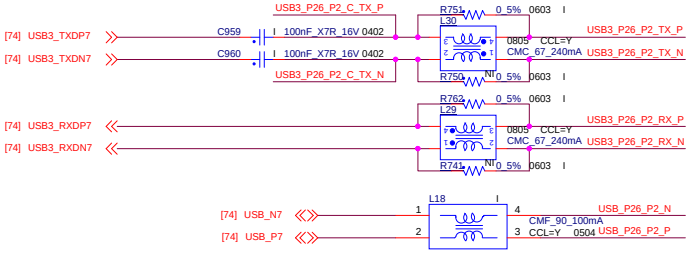
Front USB3

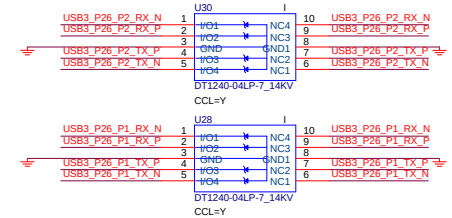


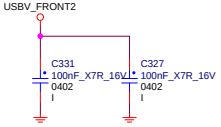


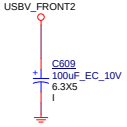












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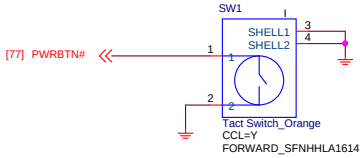
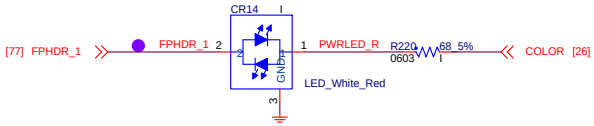
Title	F-USB3.1-REDRIVER
Size / Document Number	Custom / Rev A
Date: Wednesday, November 09, 2016	Sheet 87 of 95

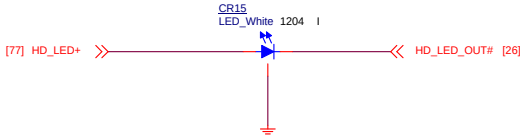
Front Power Button



Front Power LED



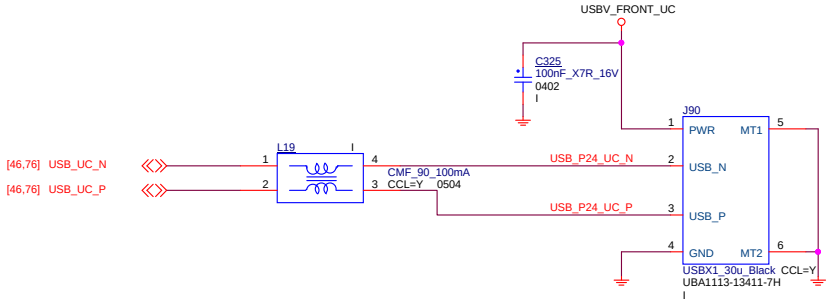
FRONT HDD LED

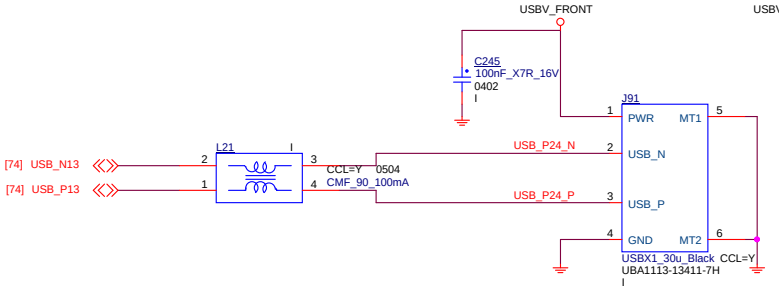


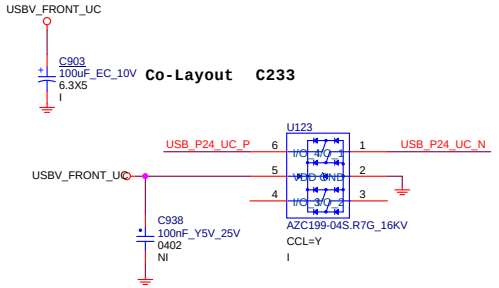
Chassis ID

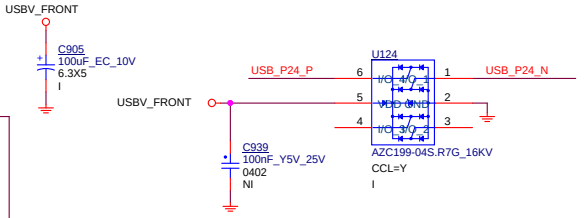
Front USB2

P24 USB 2.0 - Common Parts









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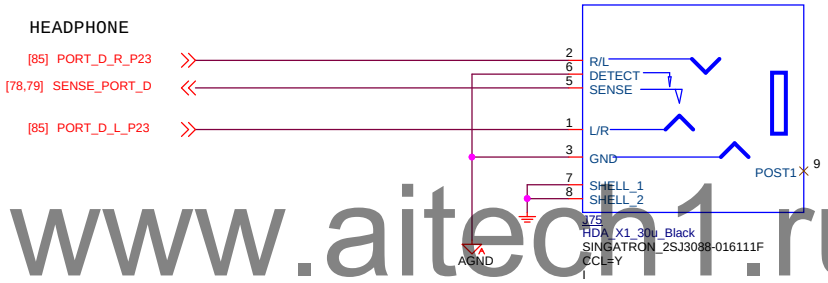
Title	F-USB2.0/F-PANEL
Size / Document Number	Rev A
Date: Wednesday, November 09, 2016	Sheet 88 of 95



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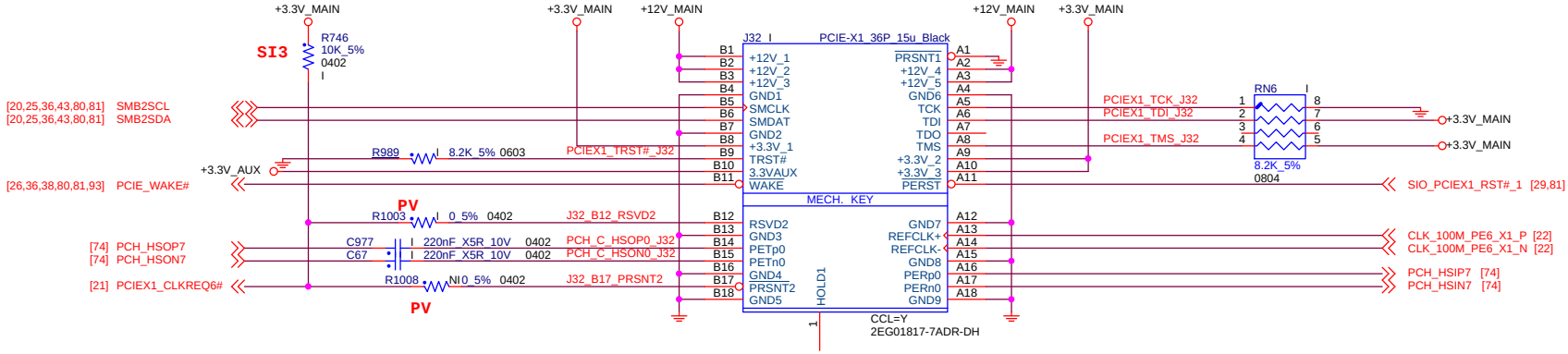
Title: F-HEADPHONE

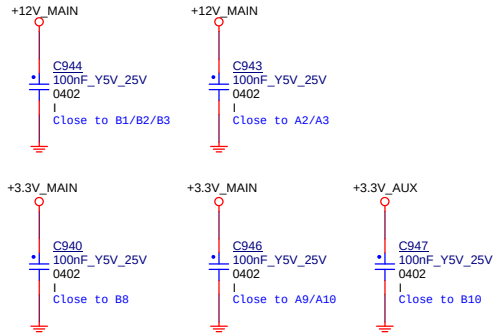
Size: Custom | Document Number | Rev: A

Date: Wednesday, November 09, 2016 | Sheet 89 of 95

PCI EXPRESS X1 SLOT3



PCI EXPRESS X1 SLOT3 Decoupling CAP



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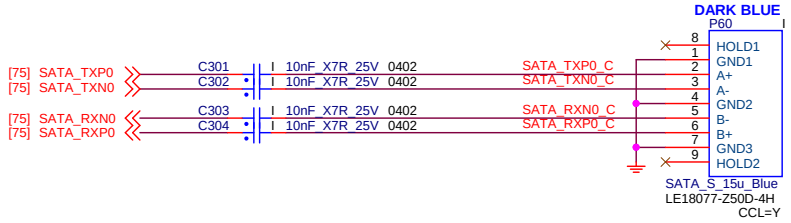
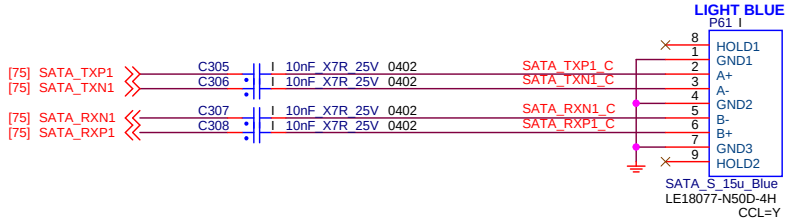
Title	PCIE - x1(SLOT3)
Size	Custom
Document Number	
Rev	A
Date:	Wednesday, November 09, 2016
Sheet	90 of 95

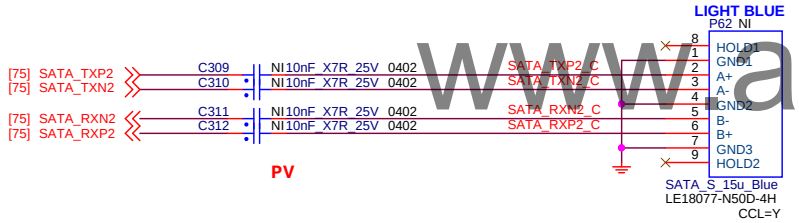
SATA Port1



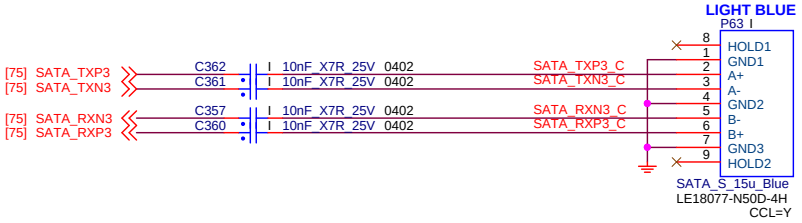
SATA Port2



SATA Port3



SATA Port4



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Title	SATA	
Size B	Document Number	Rev A
Date: Wednesday, November 09, 2016	Sheet 91 of 95	

PCB1 I

Printed Circuit Board

PCB_REV:A
CCL=Y
4-Layer PCB,Color With Green Soldermask,White Silkscreen,NPG-TL,ML1,11.844X9.6 inch,Rev:A,ROHS,HF
0101DET05-35K-H

1 2 CHECK

MTG1 NOBOM MOUNTING_HOLE MH39X80_8
MTG2 NOBOM MOUNTING_HOLE MH39X80_8
MTG3 NOBOM MOUNTING_HOLE MH35X80_8
MTG4 NOBOM MOUNTING_HOLE MH35X80_8
MTG5 NOBOM MOUNTING_HOLE MH39X80_8
MTG6 NOBOM MOUNTING_HOLE MH39X80_8
MTG7 NOBOM MOUNTING_HOLE MH39X80_8
MTG8 NOBOM MOUNTING_HOLE MH39X80_8

FM1 FM2 FM3 FM4 NOBOM NOBOM NOBOM NOBOM
FM5 FM6 FM7 FM8 NOBOM NOBOM NOBOM NOBOM

[71] VRM_PHASE3_20 TP330 NOBOM
[70] VRM_PHASE2_20 TP325 NOBOM
[70] VRM_PHASE1_20 TP326 NOBOM
[70] VRM_HGR1_20 TP327 NOBOM
[70] VRM_HGR2_20 TP328 NOBOM
[71] VRM_HGR3_20 TP329 NOBOM
[21] PCI_CLKREQ11# TP331 NOBOM

For EMI

C279 place close to MTG4
C289 place close to MTG2
C290 place close to MTG5

+5V_AUX

+VDDQ C145 100nF_X7R_16V 0402 I
+VDDQ C149 100nF_X7R_16V 0402 I

XU1_HS NI
Backplate with 8 holes
HEATSINK_CPU
HS_4H_3622X3686_TEMP

XU1-1 MH3 ILM_SH3 ILM_SH1 MH1 ILM_SH2 MH2 CCL=Y

XU1-2 1 CCL=Y

@XU1-3 LGA115X_CPU_COVER 012-1000-5377 CCL=Y

@CR14CR15 LED_Cover I

EMI CAP

M.2 2230

NUT6 I

C981 0402 100nF_X7R_16V NI VCCST_PWRGD_1V [13,21]
C989 0402 33pF_NPO_50V NI PMDOWN [10,20]
C995 0402 33pF_NPO_50V NI PMSYNC [10,20]
C990 0402 100nF_X7R_16V NI PCH_CPU_TRIGGER_IN [10,20]
C991 0402 100nF_X7R_16V NI CPU_PCH_TRIGGER_OUT [10,20]
C992 0402 680pF_X7R_50V NI THERMTRIP#_SIO [26,28]

PV Close to PCH
PV Close to CPU
PV Close to CPU
PV Close to PCH
PV Close to SIO

+VDDQ C982 100nF_X7R_16V 0402 NI
+VDDQ C983 100nF_X7R_16V 0402 NI
+VDDQ C984 100nF_X7R_16V 0402 NI

+VCCIO C993 100nF_X7R_16V 0402 I
+VCCIO C994 100nF_X7R_16V 0402 I
PV Close to R144

+VIN_+VCCIA C996 100nF_X7R_16V 0402 NI
+VIN_+VCCIA C997 100nF_X7R_16V 0402 NI
PV

USBV_LAN C986 47uF_X5R_6.3V 0805 NI
USBV_LAN C987 47uF_X5R_6.3V 0805 NI
USBV_LAN C988 47uF_X5R_6.3V 0805 NI

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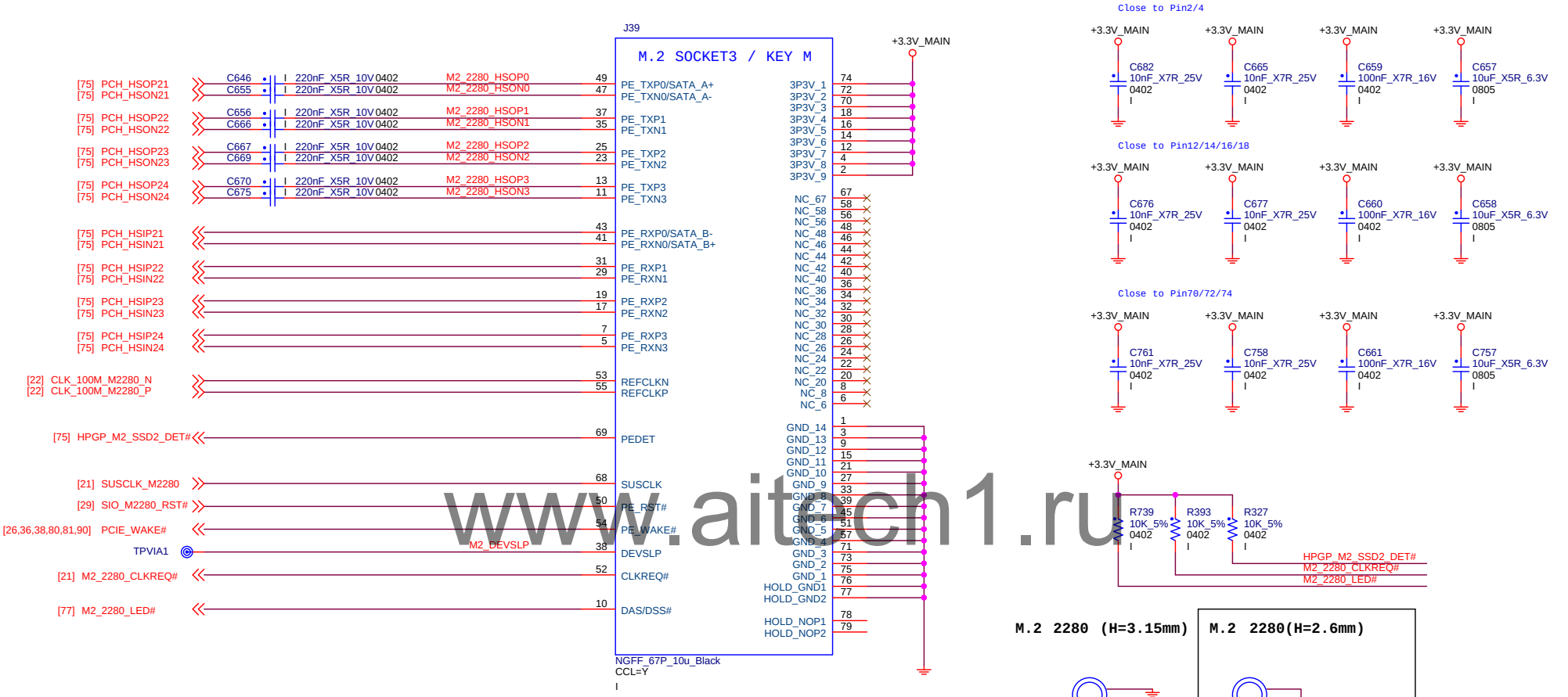
Title PCB/EMI CAP
Size B | Document Number | Rev A
Date: Wednesday, November 09, 2016 | Sheet 92 of 95

M2. 2280 - STORAGE



M.2 2280 (H=3.15mm)

M.2 2280(H=2.6mm)

SI3

DRAWN BY	FOXCONN	
Title	M.2 2280-3M-FT ONLY	
Size B	Document Number	Rev A
Date: Wednesday, November 09, 2016	Sheet 93 of 95	

Change List for DB1

0407
P41: Correct RN2 and C386 POWER TO USBV_LAN which is according to HP request
for USB and PS2 support S5 Wakeup must use the same power. SIO1291884
P22: Add R175, R176, R177, R178 as PCA rebision ID. SIO1292039
P88: Add RT11 and C158 for D8TWR VGT thermal sensor for D8TWR only. SIO1287654
P85: Add net name MIC_BIAS_INOUT_SEL for R170. Connection is correct just adjust the naming. SIO1292070

P89: Update D8TWR PCB TEMP PN to T-DT8TWR-DB1-35K-H. SIO1292076
P85: Update PJP13 Footprint to SHORTPAD_R1SX170_INNERL2. SIO1292079

0408
P37/P83: Update C350, C354 to CHEMICON_EKY-160EC3221MF111. SIO1292084
P23: Reserve R172 PD for RSMRST#. Follow Intel Check List 0.7 requirement.SIO1292089
P23: Change R159 to 20k_1% for SRTCRST#. Follow Intel Kabylake PDG requirement. SIO1292096
P29: Reserve R179 PU +3.3V_LPS for LPS_WAKE#. Follow SIO 6PCA Feature Requirement 0.3. SIO1292100
P50: Change R146 to 4.7k. Follow SIO 6PCA Feature Requirement 0.3. SIO1292102
P77: Update J10 PN to UEA1143-Q415N-4H for black color requirement. SIO1292105
P33: Update TPM PN to INFINEON_SLB9670VQ2.0FW7.40. SIO1292108

Change List for SI1 and SI2

0420
P89: Change PCB1 PN to 0101DDT01-35K-H for Andromeda. SIO1291872

0426
P41: Add R180, R181, R253, R324 for Option Card Detect#. SIO1292024

0427
P32: Set U1 BOM to NI,NI,I,I,NI,NI. Set R531 BOM to I,I,NI,NI,I,I. SIO1292019
P39/40: Experience from Basso. Add Q2 and Q19 to avoid leakage driving back from DP related device. SIO1292008

0429
P44: Add R369, R370, R383, R384 for Front Type C PD controller MOD ID. SIO1290879
P44: NI R104. Remove U6 and PD_OVP_TRIP_P1 related net. Follow Cypress Reference Circuit x7. OVP_TRIP_P1 is no longer
need. This Pin has been changed to GPIO. SIO1290879
P22: Change R176 BOM to I and Change R175 BOM to NI for PCA board revision 01. SIO1292027
P30: Remove R863, R862, R861, R436, R866, R865, R864, R504, which are PCA revision ID circuit from SIO. SIO1292039

0503
P41: Rename P81.2 to SMB_CLK_TYPEC and Rename P81.6 to SMB_DAT_TYPEC. Connection is correct just adjust the naming. SIO1292050

0504
Update Power schematic, please refer to PWR Changelist for detail
P41: Change Legacy IO Header from P54 Part reference to P74 and Change signle COM port P52 part reference to P54. SIO1293155
P13: Refer to PWR test results. NI C558, C559, C560, C912, C913, C914, C915, C561, C562. Instal C563, C564, C565, C566, C567, C557, PC661. SIO1292334

0505
P53/P21/P11: Add DP Port E connection for D4 leverage core deisgn with D8/D6. And add test point for D8D6. SIO1292897
P16/P18: Add colay symbol on DDR XMM3 and XMM1 for D4 leverage with D8/D6. And set BOM I,I,I,I,NI,NI for D8/D6 DIMM
slot and set BOM to NI,NI,NI,NI,I,I for D4 DIMM Slot. SIO1293108

0509
P27/P41/P51/P76/P78/P82/P84/P86: Change P74, P160, P54,P5,P24,J31,J32,P124,D27,D23,D24,D29,D2,P23 to CCL part. SIO1293888
P15/P16/P17/P18: Update DIMM solt PN to DB1 Build component. XMM1=XMM3 = FOXCONN_AH08827-39B10-4H and XMM2=XMM4 =
FOXCONN_AH08827-39V10-4H. SIO1293904

0510
P85: Change R239 PU power to +3.3V_LPS. SIO1287157
P21/P81/P87: Follow HP Port Map - Kabylake201605101530 to update port map. SIO1294671

0511
Update PWR Schematic. Please refer to PWR Change list for detail.

0512
P81: Change U24 and U25 to ON_ESD7504MUTAG. Refer to Skylake ESD results. SIO1295624
P80: Change P80 to FOXCONN_HLL2107-CBC2D-4H. Refer to Basso results.SIO1295626
P79/P80/P81: Refer to Skylake EMC results. Uninstall Common mode choke form Front USB3 port,
Front Type C port, Rear USB3 port, Install 0ohm bypass resistor for them. SIO1295631

0513
Update PWR Schematic. Please refer to PWR Change list for detail.
P21: Add PCI_CLKREQ11# for PCI platform leverage. SIO1295993

0517
Update 0517_1700 PWR Schematic. Please refer to PWR Change list for detail.
P52: Change P72 Connector to ACES_50185-0604C-001. SIO1297069

0518
Update 0518 PWR schematic. Refer to PWR Change list for detail
P21: Remove redundant R618 and VCORE_PG_BF path to PCH SYS PWROK. SIO1297945
P10: Remove redundant R956 PU on CPU_SELECT#. SIO1298084
P51: Change P54 to FOXCONN_HLH2077-LAB1B-4H for tail length = 2.1mm request from Factory. SIO1297951
P31: Change P74 to FOXCONN_HLH2107-LAA3B-4H for tail length = 2.1mm request from Factory. SIO1297951

0522
P85: Set R125 BOM to "I" to fix Audio diag beep sound slight issue. SIO1295426

0523
P44: Remove RN5 PU on HMSCL/SMSDA due to duplicate PU. SIO1299442
P22: Remove GND from U4.BF1 and BG2 according to Intel review feedback. SIO1298490
P20: Change R120 and R121 to 30ohm_5% according to Intel review Feedback. SIO1298490
P26: Change R680 BOM to "NI" Due to duplicate PU on R142. SIO1298490
P46: NI R148, Duplicate PU on R448 according to Intel review Feedback. SIO1298490
P44: Remove R371 PU resistor for CCG4 and Move R947 to SIO Page. SIO1298490
P9: Add D5 and Change R102 to 1.5k to fix XDP issue under Quad IO mode. SIO1298642
P32: Set U1 BOM to I,I,I,I,NI,NI. Set R531 BOM to NI,NI,NI,NI,I,I. Due to D8 series will support M.2 SSD SIO1292019

0525
Update PWR Schematic. Please refer to PWR Change list for detail.
P27/28/29/38/43/45/47/76: Change 2N7002-7-F to NXP_NX7002AK. SIO1301509

0526
P27: Change CROWBARD circuit follow HP request. R603 PWR change to +12V_MAIN and its devider circuit connect to SIO_12VIN. R521 PWR change
to +12V_ALW and its devider circuit connect to SIO_12VSB_COMP. SIO1296502

0527
Update PWR Schematic. Please refer to PWR Change list for detail.

0531
P81: Change P27 Front Type C Port map to USB Port6&7; Change P26 Front USB3 port map to 4&5; Change P60 Port map to SATA Port3; Change P63
port map to SATA Port0. SIO1294671
P9/P13/P20: Update XDP schematic. Follow Intel Kabylake RVP8 Merge XDP design. SIO1298642

0601
P81: Change U120 to ON_ESD7504MUTAG for ESD case on D8TWR Cabled FIO. SIO1303138
P44: Change R231 to 1kohm_5% for CCG4 FW cannot be read issue. SIO1302906
P81: Remove U3(3090) due to supplier confirm 3290 sample will be provided starting from SI1. SIO1303141
P36: Reserve R154 for J41 Pin B12 to Clkreq#; Reserve R395 for J31 Pin B12 to Clkreq#; Reserve R397 for J32 Pin B12 to Clkreq#; Reserve R398
for J42 Pin B12 to Clkreq#. SIO1295393

0602
P52: Update PN for P72 to ACES_50185-0604C-001. SIO1297069
Change DIODES_DMN65D8LDW-7 to CCL Part for 2nd source matrix build. SIO1303798
P21/P26: Reserve C218 for PCH_RSMRST# NMV. Add C195 for SLP_S4#_SIO NMV. Add C196 for SLP_S3#_SIO NMV. Add C209 for LPS_WAKE_R NMV. SIO1304534

0603
Update PWR Schematic. Please refer to PWR Change list for detail.
P36: Reserve R154 for J41 Pin B12 to Clkreq#; Reserve R395 for J31 Pin B12 to Clkreq#; Reserve R397 for J32 Pin B12 to Clkreq#; Reserve R398
for J42 Pin B12 to Clkreq#. SIO1295393
Update 0603_1700 PWR Schematic. Please refer to PWR Change list for detail.

0604
P21: Remove Unused PU R904, R905, R906, R907, R334, R908, R909, R335 to have more spacing for layout. SIO1304531
Change USB2.0 Common choke from INPAQ_MCM2012B900GBE to CHILISIN_MCF11T-900M-N2. New part is 0504 size. To have more space for layout SIO1304544

0606
P21: Add R406, R172, C220, R334, R335, R399, R404, Q21, Q22, R403, R405, C58, C221 as isolation buffer ciurcit to avoide the
coupling on VCCST_PWRGD and PCH_PWROK. SIO1302948
Update 0606_1100 PWR Schematic. Please refer to PWR Change list for detail.
P9: Update XDP schematic. Follow Intel Kabylake RVP8 Merge XDP design. SIO1298642
P10: Set R47 BOM to "NI,NI,NI,NI,I,I" due to only D4 need to use eDPI to VGA. SIO1304922
P41: Set P160 BOM to "I,I,NI,NI,I,I" due to D6 will use 2x2 SATA PWR Connector. SIO1304920
P85: Change Q14, Q2, Q19 to CCL for 2nd source qual. SIO1305210

0607
P45: Change R103 and R549 to 0 ohm resistor for SMBus SI testing with AV2 failure. SIO1305213
P85: Change C126, C133, C134, C135 to 10uF_X5R_16V for Rear LineOut, Front LineIn and Front MicIN. SIO1305147
P36: Change RN3 to R415, R416, R418 for better laytout routing. SIO1305356

0608
P45: Change R103 and R549 to 100 ohm resistor for SMBus SI testing with AV2 failure. SIO1305213

0612
P25: Add R419=0ohm RES but NI between SX_EXIT_HOFF# and SIO Pin92. SIO1306205
P89: Reserve C219, C222, C224 for D8TWR EMI. SIO1306387
P44: Change R231 and R392 to 1kohm_5% for CCG4 FW cannot be read issue. SIO1302906

0613
P21: Add R406, R172, C220, R334, R335, R399, R404, Q21, Q22, R403, R405, C58, C221 as isolation buffer ciurcit to avoide the coupling on
VCCST_PWRGD and PCH_PWROK. SIO1302948
P78/P45: Change U4.AL45 to HPGP_LANCABLE_DET# and connect to new adding Q28, R420 and R421 for HP Request to add Lan cable dectec feature.
SIO1306206
P85: Per Conexant review feedback. Change U13.Pin30 Power trace from +3.3V_MAIN to +3.3V_AUX and Change R170 to AVDD_3.3. SIO1307068
P21: Remove Unused component R904, R905, R906, R907, R334, R908, R909, R335, R254, RT9 to have more spacing for layout. SIO1304531

0614
Update 0613_2000 PWR Schematic. Please refer to PWR Change list for detail.
P52: Change NUT2 and NUT3 to RONNIE_55-20220-23 for the latest stand off requirement on Rear Daughter Card. SIO1307202
Set D1, D28, D30 to CCL for 2nd source qual. SIO1305210
P36: Change J42 to FOXCONN_2EG73217-73W2-4H. SIO1295393

0615
P34: Follow HP's request to chnage SHD SPI Topology. SIO SHD SPI Interface is treated as 2nd flash device and follow Intel PDG for routing.
SIO1308015
P44: Change R392 to +5V_AUX according to Vendor review Feedback. SIO1308163
P88: Implement on board ambient sensor and reserve cabled sensor Header (P128A and P128B) for Andromeda. SIO????????

0616
P43: Change R361 = 0ohm, R426 = 10K PD on Q38.G for SIO1293830

0621
P28: Change RT12 to NI for Apus. SIO1308726
P86: Change D3, D4, D35, PQ312, Q267, Q39, Q28, Q21, Q22 to CCL Part for 2nd source qual. SIO1305210
Update 0621 PWR Schematic. Please refer to PWR Change list for detail.

0622
P27: Change R603 to 11.8K_1%, R641 to 1.78K_1%, R521 to 287K_1%, R522 to 59K_1% for Updated Crowbar circuit. SIO1296502

0624
P27: Change R523 to 1k_1% SIO1296502

Change List for SI3

0718
P45: NI R612 and Instal R242 to fix LAN leakage in LPS state. SIO1318234
P36/83/84: Add R427, R430, R431, and R433 series Resistor = 0ohm between CLKREQ and PCIe PRSNT2# Pin. SIO1311029
P13:Change Q287 to APEC_AP2N025N as main source from 2nd source. SIO1311035
P21: Change R334 to 47ohm and R399 to 1kohm. SIO1302948

0719
Update PWR Schematic. Please refer to PWR Change list for detail.
P26: Rename SIO_PIn65 net name from SIO_GPIO84 to HPGP_IMON_NEXTX. SIO1318015
P42: Change E23 Platform Debug Pin13 connection to SIO.PIN91 "HPGP_PSU_ID_SEL". Follow SRB 4.0. SIO1318726

0720
Change PCB1 PN to 0101DDT02-35K-H for SI3. SIO1318959
Change U4 PCH PN to "INTEL_GL82Q270-QL0M" and BOM to "I,I,I,I,NI,NI" for SI3. SIO1318958
P52: Add patch solution about Rear OPT card has no display issue which is to add R435, R436 = 2.2kohm and pull-up with +3.3V_MAIN on
DDPD_CTRLCLK and DDPD_CTRLDATA respectively. SIO1317080
Update PWR Schematic. Please refer to PWR Change list for detail.

0721
Change USB2.0 CMC main source PN to TDK_MCZ1210AH900L2TA0G. It's from 2nd source. SIO1319463
Change Display port ESD PN to DT1240-04LP-7 to merge with USB3 ESD. SIO1319465
P31: Change Legacy IO Header part reference to P75. SIO1319462

0725
Update PWR Schematic. Please refer to PWR Change list for detail.
P82: Andromeda only. Change P61 to SATA Port1 and P63 to SATA port3. SIO1315987

0726
P38/P79/P80/P81: Remove USB2.0 CMC colay Resistor to fix soldering issue. SIO1321010.

0727
P21: Install C218 to Fix PCH_RSMRST# NMV Issue. SIO1304534
P38: Change R351 to 22ohm and C751 to 1nF to fix M2230_CL_RST# Overshoot and Undershoot issue. SIO1321472
P26: Add two 0ohm resistor (R28, R29) on PWRGD_30MS and place close to SIO and PQ604 as well as one Cap (C225) reserve on PWRGD_30MS near PQ604
for noise on PWRGD_30MS. SIO1321579

0728
P84: Add colay footprint JS42 with J42. SIO1321721
P85: Change C273 and C274 to 10uF_X5R_16V for Rear LineIn port failed on THD+N@20Hz. SIO1320849
Update PWR Schematic. Please refer to PWR Change list for detail.

0729
P85: Add R35 and R36 for AVDD_HP Power connection reserve. SIO1307068

0801
Update PWR Schematic. Please refer to PWR Change list for detail.
Core design Page, Page1-54, add projects application status

0802
P97 Add notice wording for C2, R342, R365 in XDP page. SIO1298642
Change P54 naming to D8D8_CLINK_Header
Update chipset sku in Index page for D400 series

0803
P36: R427 NI, R154 I for x16 J41 CLKREQ# to B12. SIO1311029 and SIO1295393
P83: R430 NI, R395 I for x1 J31 CLKREQ# to B12. SIO1311029 and SIO1295393
P83: R431 NI, R397 I for x1 J32 CLKREQ# to B12. SIO1311029 and SIO1295393
P83: R433 NI, R398 I for x4 J42 CLKREQ# to B12. SIO1311029 and SIO1295393
P34/P13/P28/P39: Change E1, E2, E15, E21, E49 PN to PINREX_210-HB1-02HB01 from 2nd source. SIO1323699

0804
Update PWR Schematic. Please refer to PWR Change list for detail.

0805
Update PWR Schematic. Please refer to PWR Change list for detail.
P80/P81: NI R570, R569, R567, R568, R565, R566, R563, R564, R741, R762, R751, R750, R753, R752, R754, R755 and Install L59, L58, L57, L56,
L29, L30, L31, L32. for RF 2.4GHz and 5GHz performance for front USB3 and Type C port. SIO1324891

0808
P85: Change R36 to "I" and R35 to "NI" for 0805 HP request to change Codec Pin30 to +3.3V_MAIN Path. SIO1307068

0810
P36: R427 I, R154 NI for x16 J41 CLKREQ# to PRESENT# PIN. SIO1311029 and SIO1295393
P83: R430 I, R395 NI for x1 J31 CLKREQ# to PRESENT# PIN. SIO1311029 and SIO1295393
P83: R431 I, R397 NI for x1 J32 CLKREQ# to PRESENT# PIN. SIO1311029 and SIO1295393
P83: R433 I, R398 NI for x4 J42 CLKREQ# to PRESENT# PIN. SIO1311029 and SIO1295393
P34: Change R254 to 68ohm to fix TPM SPI Clock without enough margin on D8/D4 FSR testing and failed FSR results on D6. SIO1326346
P20: Change R880 BOM from NI to I for XDP/DCI support. SIO1326396
Update PWR Schematic. Please refer to PWR Change list for detail.
P45: Change U10 Lan Chip PN to WGI219LM[SLKJ3] for SI3 Build. SIO1326375

Change List for PVT

0830
P81: Reserve D6 NXP_PTVS20VS1UR TVS @ NXP3290 Output for surge protect. SIO1325995
P81: Change C390, C426 to 10nF_X7R_50V to support higher voltage when surge happened. SIO1325995
P81: Change C425 to 100nF_X7R_50V to support higher voltage when surge happened. SIO1325995
P81: Change C391 to 10uF_X5R_16V to support higher voltage when surge happened. SIO1325995
P81: Change C392 to 100nF_X7R_16V to support higher voltage when surge happened. SIO1325995

0901
P26: Delete R28, R29 series 0ohm resistor and short the net directly. SIO1321579.
P20: Change Board Revision ID to "10" for PVT1. R175 Install; R176 NI; R177 NI; R178 Install. SIO1334054.

0902
P89: Change PCB PN to 0101DDT03-35K-H for PVT. SIO1334326
P34: Change R254 to 0ohm. SIO1326346

0908
P89: Add C140 and C173 for PMDOWN and PMSYNC respectively. SIO1332631
P89: Reserve C177 and C182 for PCH_CPU_TRIGGER_IN and CPU_PCH_TRIGGER_OUT respectively. SIO1332631
P89: Add C185 and C229 stiching CAP for Moat Crossing of PMDOWN, PDSYNC, PCH_CPU_TRIGGER_IN and CPU_PCH_TRIGGER_OUT. SIO1332631
P23: Delete R316 and R367 and U4.F39, U4.F43 short to GND directly. Follow Intel CRB 1.0. SIO1335615

0909
P25: Add Colay Symbol and footprint for SIO15 New part but NI. SIO1332648
Update PWR Schematic. Please refer to PWR Change list for detail.

0912
P88: Remove P128 and R100. PVT/EEP/MP will be no longer to supprot Cabled Ambient Sensor. SIO1287654

0913
Change PN:BAT54C-7-F, PN:BAT54A-7-F, D5 Location, PN:NX7002AK, PN:DMN65D8LDW-7, PN:P8503BMG,
PN:MMBT3906-7-F, PN:MMBT3904-7-F, Header E18 to Non-CCL Part. SIO1347590

0914
P89: NI C140, C173. SIO1332631
Update PWR Schematic. Please refer to PWR Change list for detail.

0919
P41: Change C441 to RUBYCON_16ZLH470MHFCCR8X11.5 which is higher performance due to thermal issue. SIO1348712
Update PWR Schematic. Please refer to PWR Change list for detail.
P84: NI J42, Install JS42 = FOXCONN_2EG73217-73W4-4H which is Standard PCIex4 slot. SIO1311029 and SIO1348750
P36: R427 NI, R154 I for x16 J41 CLKREQ# to B12. SIO1311029 and SIO1348750
P83: R430 NI, R395 I for x1 J31 CLKREQ# to B12. SIO1311029 and SIO1348750
P83: R431 NI, R397 I for x1 J32 CLKREQ# to B12. SIO1311029 and SIO1348750
P84: R433 NI, R398 I for x4 J42 CLKREQ# to B12. SIO1311029 and SIO1348750

0920
P81: Install D6 NXP_PTVS20VS1UR TVS @ NXP3290 Output for surge protect. SIO1325995
P26: NI R153 and Keep PR820 "I" due to double PU on PME_IN#/HPGP_PSU_ID_STATUS. SIO1349113

Change List for PV2

P89: Change PCB PN to 0101DDT04-35K-H for PVT2. SIO1351897

P29->P76: Move the PWR LED and HDD LED circuit from core design to page76 and
Change R211 to 2.87kohm and R143 to 3.9kohm for SID request FIO LED brightness
issue.SIO1365766
Update PWR FLOW

1026
P20: NI R175 and Install R176 for PV2 PCA Revision ID=11. SIO1368197

Change List for MP

1027
P34: Change U19 and U68 to SMD type for MP. SIO1351859

P20: Change PCA revision ID to "00" for MP. R178 NI, R177 I, R176 NI,
R175 I. SIO1351874

P9: Change XDP header P4 Footprint to "HMS2X30CZ_MVB_NP" for MP. SIO1351889

P45: Change U10 Lan chip PN to WGI219LM[VER.A0,SLKJ2] for MP. SIO1352404

P44: Update CCG4 is HF product information for "CYPD4125-40LQXIT" and update
Foxconn PN to 210823C00-244-H For MP. SIO1364372

P89: Change PCB PN to 0101DDT05-35K-H and change the description for
soldermask color to Green and Silkscreen Color to White for MP. SIO1368663

P25: Remove SIO Colay symbol and footprint for MP. SIO1348602

P85: Update U13 s HF product information for "CX20632-31Z" and update
Foxconn PN to 2103DDG00-438-H For MP. SIO1368675

Update U4 PCH PN to GL82Q270_A0,SR2WE for D8/D6 MP. SIO1368677

1031
P81: Update U54 NXP_NX5P3290UK is HF product information for "NX5P3290UK" and update
Foxconn PN to 320244P00-031-H For MP. SIO1369350

DB1

P65. Connect 12V_PG_25ms to PQ751.G1[SIO1286473]
P65. Change PQ751 to PQ751A and PQ751[SIO1286473]
P65. Add PR762, delete PR753[SIO1286473]
P58. Delete PJP911,PJP912. add PC925 and set NI[SIO1286474]
P58. Set PL980 to I[SIO1286474]
P61. DeletePJP511,PJP512. add PC522 and set NI[SIO1286474]
P61. Add PL512[SIO1286474]
P63. Delete PJP479. add PC470 and set NI[SIO1286474]
P63. Set PL470 to I[SIO1286474]
P67. Delete PJP607, add PC616 and set NI[SIO1286474]
P67. Add PL607 [SIO1286474]
P68. Delete PJP654, add PC664 and set NI[SIO1286474]
P68. Add PL652 [SIO1286474]
P55. Change PR808 from 100k ohm to 10k ohm and set NI [SIO1286477]
P55. ChangePR805 from 49.9k ohm to 20k ohm [SIO1286477]
P55. Set PR807,PR804,PR803,PR180 to NI[SIO1286477]
P55. Set PR801,PR806 to I[SIO1286477]
P57. Change PR858 from 25.5k ohm to 45.3k ohm [SIO1286486]
P57. Set PC851,PC850,PR852,PR859 to NI[SIO1286486]
P57. Set PQ851,PR854 to I[SIO1286486]
P69. Change PR124 from 63.4k ohm to 80.6k ohm (Imax set from 79A to 100A) [SIO1286488]
P69. Change PR134 from 24.9k ohm to 30.9k ohm [SIO1286488]
P56. Change PR839 from 261k ohm to 31.6k ohm [SIO1286481]-Andromeda
P56. Change PR824 from 78.7k ohm to 60.4k ohm [SIO1286481]-Andromeda
P56. Change PR828 from 261k ohm to 187k ohm[SIO1286521]-Carina/Crux

SI1

P56. Change PR824 to non-lead free.[SIO1292981]-Andromeda
P56. Change PR124 to non-lead free.[SIO1292981]-Andromeda
P69. PC661 to I for intel PAL requirement[SIO1292334]
P60. Add PR164 to parallel with PC132 [SIO1292159]
P56. Set PR828,PR829,PR830,PR831,PQ820,PQ821 to NI[SIO1293871]-Apus
P58. Change PR912,PR921 package size from 0805 to 1206[SIO1289106]
P63. Change PR484,PR479 package size from 0805 to 1206[SIO1289106]
P60. Change PR665,PR650 package size from 0805 to 1206[SIO1289106]
P70. Change PR210,PR212,PR222,PR221 package size from 0805 to 1206[SIO1289106]
P71. Change PR230,PR233 package size from 0805 to 1206[SIO1289106]
P72. Change PR259,PR255,PR268,PR262 package size from 0805 to 1206[SIO1289106]
P55. Add PD800,PC800 [SIO1295099]
P55. Change PQ80040 to PQ800 and PQ801[SIO1295099]
P69. Change PR164 from 6.19k ohm to 5.1k ohm[SIO1295701]
P69. Change PC122 from 1.5nF to 1.2nF[SIO1295701]
P69. Change PR132 from 174k ohm to 180k ohm[SIO1295701]

05/17/2016:

P65. Add PR769,PC754,set PC752 to I[SIO1297648]
P58. Change PC918 from 1uF to 100nF[SIO1297648]

05/18/2016:

P67. Delete PR610 [SIO1301221]
P55. Change PR800 from 10k ohm to 100k ohm[SIO1286477]
P55. Change PR805 from 20k ohm to 200k ohm[SIO1286477]

05/24/2016:

P58. Delete PQ836,PQ946[SIO1301245]
P72. Delete PCE284[SIO1301261]
P73. Delete PC6473,PC6477[SIO1301245]
P60. Change the Vin of +1.8V_AUX rail from +5V_AUX to +3.3V_AUX[SIO1301296]

05/25/2016:

P55,56,57,62,63,64,67. Change PQ800,PQ801,PQ820,PQ821,PQ851,PQ563,PQ477,PQ310,PQ311,
PQ711,PQ713,PQ714,PQ451,PQ840,PQ681,PQ682,PQ683,PQ684,PQ685 from 2N7002-7-F to BX7002AK[TBD]
P63. Delete one choke PL470, add two bead PL470,PL471[SIO1301245]

05/31/2016:

P68. Set PC653 from NI to I[TBD]
P68. Set PR666 to I, change PC662 from 33pF to 100pF[TBD]
P63. Change PR482 from 39k ohm to 470k ohm[TBD]
P62. Change PC576 from 22pF to 82pF[SIO1303514]
P58. Change PR929 from 15.8k ohm to 15.4k ohm[SIO1303541]

06/03/2016:

P69. Delete VCORE_PG buffer circuit[SIO1302948]

06/06/2016:

P67. VCORE_PG circuit modify[SIO1302948]

06/13/2016:

P55. Change PR805 from 200k ohm to 33.2k ohm[SIO1307052]
P55. Add PR802 and set NI[SIO1307052]
P55. Change PD800 from 1N4148WS-7-F to BAV70 and set NI[SIO1307052]
P55. Change PC800 from 100nF to 1nF[SIO1307052]
P63. Set PR516 to NI, set PR511 to I[SIO1307055]
P67. Set PR688 to NI, set PR610 to I[SIO1307055]
P67. Set PC263 to I[TBD]
P56. Set PR829,PR830 to I[SIO1307053]

06/21/2016:

P.64 Set PQ312 to CCL(SIO1305210)

SI3

P55. Delete PR807,PQ800 and set PD800,PR802 to I [SIO1318015]
P56. Delete PR829,PR830,PR831,PQ820[SIO1318036]
P57. Add Over current circuit[SIO1318492]

07/25/2016:

P67. Remove PC604(SIO1325853)
P68. Remove PC654(SIO1325853)

07/27/2016:

P57. Change PU900 from RICHTEK_RT6576EGQW to RICHTEK_RT6575BGQW(SIO1321498)

08/01/2016:

P57. Change PD800 from BAT54CLT1G to BAT54C-7-F(SIO1318015)

08/03/2016:

P61. Change PR529 from 10k ohm to 24.9k ohm(SIO1322369)
P61. Change PR526 from 2.55k ohm to 7.5k ohm(SIO1322369)
P52. Change PR575 from 43k ohm to 53.6k ohm(SIO1323972)
P57. Change PU900 from RICHTEK_RT6575BGQW to RICHTEK_RT6575BGQW(2)(SIO1321498)

08/05/2016:

P55. Change PR850 to 422k ohm, PR860 to 1M ohm,PR862 and PR864 to 100k ohm(SIO1318492)
P61. Change PR529 from 24.9k ohm to 28.7k ohm(SIO1322369)

PV

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Title	VCORE Controller
Size	D
Document Number	
Rev	A
Date:	Wednesday, November 09, 2016
Sheet	95 of 95